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A Survey on Low Power Clock Distribution Networks Using Flip Flops

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***Abstract*—** In this paper we discuss about various low power clock distributions with an example. Many papers are taken for the survey and its advantages and disadvantages are discussed. In particular one to many clock distributions are discussed.

***Keywords*—** Clock distribution network, Flip-flop, Low power consumption.

I. INTRODUCTION

Power is a primary concern in all sort of circuits. Clock distribution networksare essential element of a synchronous and non-synchronous digital circuit and a significant power consumer. Low-power design has become quite critical in synchronous application. Current mode is used to draw attention to some kind of special dependence on currents as signals. Researchers have demonstrated that themajor consumers of this power are global buses, clock distribution networks (CDNs), and synchronous signals in general. In addition to power, interconnect delay poses a major obstacle to high-frequency operation. Technology scaling reduces transistor and local interconnect delay while increasing global interconnect delay. Previous CM schemes have been used for commonly, off chip signals. Standard logic signals, however, have remained VM to benefit from the low static power of CMOS logic. Portable electronic devices require long battery life which is obtained by utilizing low power components. Major consumers of the power are global buses, clock distribution networks (CDNs), and synchronous signals in general. The clock distribution network consumes considerable amount of power in synchronous digital systems.

The CDN's delivers the clock signal. It is the Important part of synchronous circuits to ensure the availability of the clock signal at each flip flops across the integrated circuit. Consumes large amount of total power in synchronous systemGate diffusion input (GDI)a new technique of low-power digital combinatorial circuit design is described. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. Performance comparison with traditional CMOS and various pass-transistor logic design techniques is presented.

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The different methods are compared with respect to the layout area, number of devices, delay, and power dissipation. Issues like technology compatibility, top-down design, and pre-computing synthesis are discussed, showing advantages and drawbacks of GDI compared to other methods. Several logic circuits have been implemented in various design styles

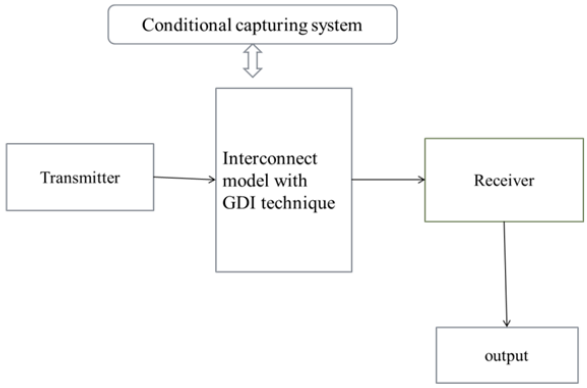

Fig 1: Clock Distribution Network

Fig1 represents the Conditional capturing system which is used to minimize power at CDNs. In this scheme the GDI technique is used to transmit the clock signal. There is a two receiver circuits are used to get an output with reduced skew. The amplifier based receiver and GDI receiver.Buffer is used as an interconnect model in this system.

S. NO	TITLE	DESCRIPTION
1	Low swing on-chip signaling techniques: Effectiveness and robustness[2].	This paper reviews a number of low-swing on-chip interconnect schemes and presents a thorough analysis of their effectiveness and limitations, especially on energy efficiency and signal integrity.
2	Physical design of a fourth-generation powerghz microprocessor [3].	The fourth-generation POWER processor chip contains 170M transistors and includes 2 microprocessor cores, shared L2, directory for an off-chip L3, and all logic needed to interconnect multiple chips to form an SMP.
3	Analytical modeling and characterizationof deep-sub micrometerinterconnect [4].	An approach to measuring femto-Farad level wiring capacitances is presented that is based on the concept of supplying and removing charge with active device.
4	High speed current-mode Signaling circuits for on-chip interconnects [5].	This paper presents three current-mode circuits for high-speed signal propagation across long on-chip busses.

5	Revisiting automated physical Synthesis of high-performance clock networks [6].	High-performance clock distribution has been a challenge for nearly three decades. During this time, clock synthesis tools and algorithms have strove to address a myriad of important issues helping designers to create faster, more reliable, and more power efficient chips.
6	An MOS current mode logic (MCML) circuit for low-power sub-GHz processors [7].	MOS Current Mode Logic (MCML) is one of the most promising logic style to counteract power analysis attacks. Unfortunately, the static power consumption of MCML standard cells is significantly higher compared to equivalent functions implemented using static CMOS logic.
7	Current-mode techniques for high-speed VLSI circuits with application to current sense amplifierfor CMOS SRAM's[8].	The speed of VLSI chips is increasingly limited by signal delay in long interconnect lines. A simple analysis shows that majorspeed improvements are possible when using current-mode rather than conventional voltage-mode signal transporting techniques.
8	A variation tolerant current-mode signaling scheme for on-chip interconnects[9].	Current-mode signaling (CMS) with dynamic overdriving is one of the most promising schemes for high-speedlow-power communication over long on-chip interconnects.
9	A low powerCurrent-mode clock distribution scheme for multi-GHz NoCbasedSoCs[10].	Performance of System-on-Chips (SoC) is limited by rising delays and noise in buses and point-to-point interconnects. This also has a profound impact on the clock distribution network.
10	A low-power low-skew current-mode clock distribution network in 90 nm CMOS technology[11]	A current-mode clock distribution network (CM- CDN) for low-power low-skew on-chip clock distribution is presented in this paper. A novel low-power current-mode receiver circuit with common-mode correction for the CM-CDN is also presented.

II. CONCLUSION

The further work in this paper is the Conditional Data Mapping Flip flop will be adds with Gate diffusion input. Then the proposing technique is much helpful for skew and latency reductions with more efficient way.Automatically the power may be reduced.

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