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A TRUNCATED CONTROL ASIC SCHEME FOR WIRELESS CRITERIONS

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Abstract — Now a days wireless communication plays major role in the world , make us relax from the overhead of cable .in this communication plays major role. CDMA is one of the emerged technology in the mobile communication .In this paper, a low power ASIC design of pseudo noise code synchronization for wideband code-division multiple access (WCDMA),CDMA 2000 and IEEE 802.11g systems is proposed. In addition to this three kinds of low power techniques such as power management, absolute weighted magnitude calculation and spurious power suppression adder is applied.

Keywords — WCDMA, low power methods, ASIC.

I. INTRODUCTION

Presently WCDMA, CDMA2000 and 802.11 g system receive a great deal of attention in wireless communications. This paper is divided into three parts such as code synchronizations for three different systems, asic architecture, and low power technique implementation. In WCDMA, a three-stage code synchronization process is implemented in 3 GPP standards, including slot synchronization, frame synchronization with code group identification and scrambling code identification. In CDMA 2000, a pilot channel is spread by a PN code with cell-specific code phase to help timing synchronization between mobile and base stations. In 802.11g, a Barker code is applied to detect bit boundary before packet identification.

The main Theme of this paper is to reduce power in the integrated synchronizer for multistandards which is implied as Asic.

II. TECHNOLOGIES USED

A.WCDMA

W-CDMA (Wideband Code Division Multiple Access) is a wideband spread-spectrum channel access method that utilizes the direct-sequence spread spectrum method of asynchronous code division multiple accesses to achieve higher speeds and support more users compared to most time division multiple access (TDMA) schemes used today. The term "W-CDMA" is also used to refer to the standard data interface used by the UMTS mobile communication system, W-CDMA (UMTS).Code Division Multiple Access communication networks have been developed by a number of companies over the years, but development of cell-phone networks based on CDMA (prior to W-CDMA) was dominated by Qualcomm. Qualcomm was the first company to succeed in developing a practical and cost-effective CDMA implementation for consumer cell phones: its early IS-95 air interface standard, which has since evolved into the current CDMA2000 (IS-856/IS-2000) standard. Qualcomm created an experimental wideband CDMA system called CDMA2000 3x which unified the W-CDMA (3GPP) and CDMA2000 (3GPP2) network technologies into a single design for a worldwide standard air interface. Compatibility with CDMA2000 would have beneficially enabled roaming on existing networks beyond Japan, since Qualcomm CDMA2000 networks are widely deployed, especially in the Americas, with coverage in 58 countries as of 2006. However, divergent requirements resulted in the W-CDMA standard being retained and deployed. Despite incompatibilities with existing air-interface standards, the late introduction of this 3G system, and despite the high upgrade cost of deploying an all-new transmitter technology, W-CDMA has been adopted and deployed rapidly, especially in Japan, Europe and Asia, and is already deployed in over 55 countries as of 2006.

B.CDMA 2000

CDMA2000 (also known as IMT Multi -Carrier (IMT-MC)) is a family of 3G mobile technology standards, based on CDMA, to send voice, data, and signaling data between mobile phones and cell sites. The set of standards includes: CDMA2000 1X, CDMA2000 EV-DO Rev. 0, CDMA2000 EV-DO Rev. A, and CDMA2000 EV-DO Rev. B All are approved radio interfaces for the ITU's IMT-2000. CDMA2000 has a relatively long technical history and is backward-compatible with its previous 2G iteration IS-95 (cdma One). In the United States, CDMA2000 is a registered trademark of the Telecommunications Industry Association (TIA-USA).Leading performance ,Efficient

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use of spectrum, Support for advanced mobile services, Devices selection: Seamless evolution path, Flexibility are key features of CDMA2000.

C.802.11g

IEEE 802.11g-2003 or 802.11g is an amendment to the IEEE 802.11 specification that extended throughput to up to 54 Mbit/s using the same 2.4 GHz band as 802.11b. This specification under the marketing name of Wi-Fi has been implemented all over the world. The 802.11g protocol is now Clause 19 of the published IEEE 802.11-2007 standard.802.11g was the third modulation standard for Wireless LAN. It works in the 2.4 GHz band (like 802.11b) but operates at a maximum raw data rate of 54 Mbit/s, or about 19 Mbit/s net throughputs (identical to 802.11a core, except for some additional legacy overhead for backward compatibility). 802.11g hardware is fully backwards compatible with 802.11b hardware. Details of making b and g work well together occupied much of the lingering technical process. In an 802.11g network however, the presence of a legacy 802.11b participant will significantly reduce the speed of the overall 802.11g network. The modulation scheme used in 802.11g is orthogonal frequency-division multiplexing (OFDM) copied from 802.11a with data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbit/s, and reverts to CCK (like the 802.11b standard) for 5.5 and 11 Mbit/s and DBPSK/DQPSK+DSSS for 1 and 2 Mbit/s. Even though 802.11g operates in the same frequency band as 802.11b, it can achieve higher data rates because of its heritage to 802.11a.

III. CODE SYNCHRONIZATION OF TECHNOLOGIES

A. WCDMA

In WCDMA, the code synchronization is divided into a three stage process Primary synchronization code, Secondary synchronization codes have to be identified by active correlator. Scrambling code is identified by ballot machine.

Stage 1 has to detect a 256-chip primary synchronization code (PSC). Generally, the matched filter is used to detect the slot boundary, and the correlation results are further accumulated for 15 slots to improve the signal-to-noise ratio (SNR).

Stage 2, one of 16 secondary synchronization codes (SSCs) has to be identified by active correlator for further comma-free Reed–Solomon decoding.

Stage 3, one of eight complex-valued scrambling codes is identified as the cell-specific scrambling code by ballot machine. Fig. 1 shows the generalized model for the three stages. First, input data are correlated with local generated PN code sequence. Then, correlation results are calculated and accumulated, and the maximal result is identified as the desired timing or the local PN code is identified as the desired one by the peak detector.

B.CDMA 2000

In CDMA2000, Pilot channel is spread by a PN code with length of 32 768 chips. It is not necessary to detect all 32 768 chips. According to [10], there is a tradeoff between hardware Complexity and correct detection rate. We decide to detect 128 chips of the PN code in a CDMA2000 system to achieve the hardware efficiency as well as the detection rate. Fig. 2 shows the generalized model.

C.802.11g

In 802.11 g, bit boundary is identified through Barker code detection. Accordingly, an 11-chip detection of Barker codes is applied to 802.11 g code synchronization. A synchronization field-matched filter is employed to calculate the correlations between and Barker codes. When the peak detector generates periodic peak values, Barker codes are located. Fig. 3 shows the generalized model.

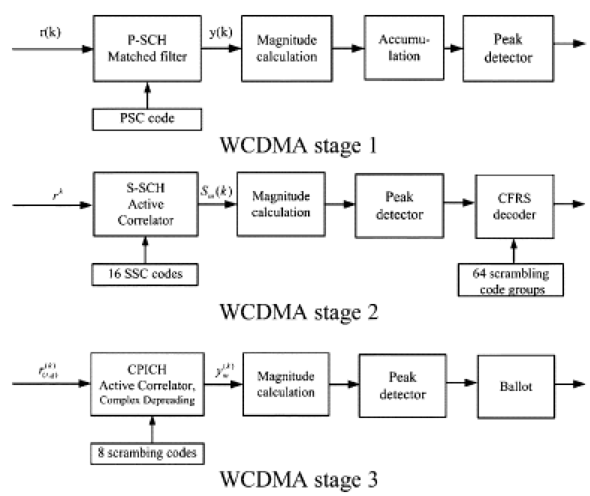

Fig. 1. Generalized model in WCDMA synchronizations.

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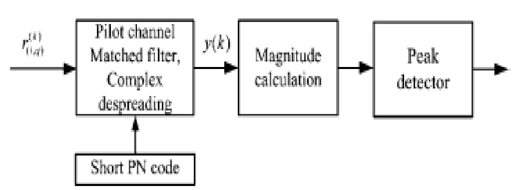

Fig. 2. Generalized model in CDMA2000 synchronization.

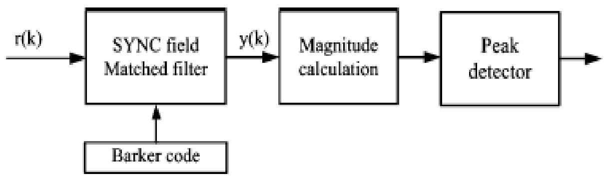

Fig. 3. Generalized model in 802.11 g synchronization.

IV. DESIGN METHODOLOGY

According to the models of Figs. 1–3, the integrated synchronizer for WCDMA, CDMA2000, and 802.11 g is generalized, and the overall model is shown in Fig. 4. Input data are correlated. With local generated PN-code sequences. Then, correlation results are calculated and accumulated, and the peak result is identified as the desired timing or the local PN code is identified as the desired one. Note that only necessary hardware blocks in this generalized model are enabled when operating in different systems.

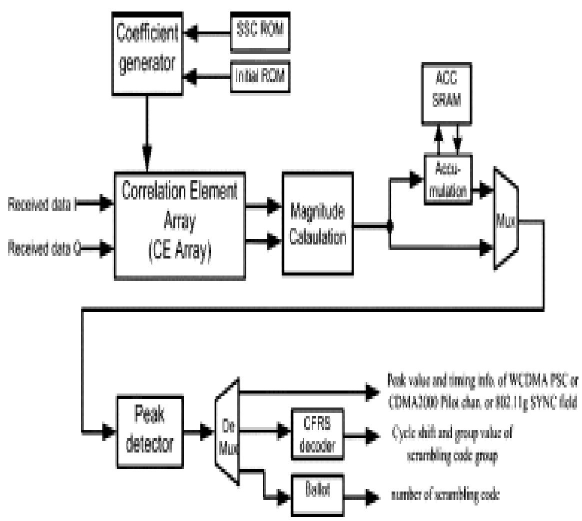

Fig. 4. System architecture.

1) Correlation Element Array

It is composed of 16 rows, each row include 16 CE's So CE Array contains 256 CE's It configured to work in 2 modes

Active mode:

partial results are fed back to its input to execute self accumulated correlations.

Passive mode:

2. Serially linked CE's form a matched filter. 1. 256 CE's are linked into chain. {Partial results will come from left hand CE and it will pass the new result to right}.

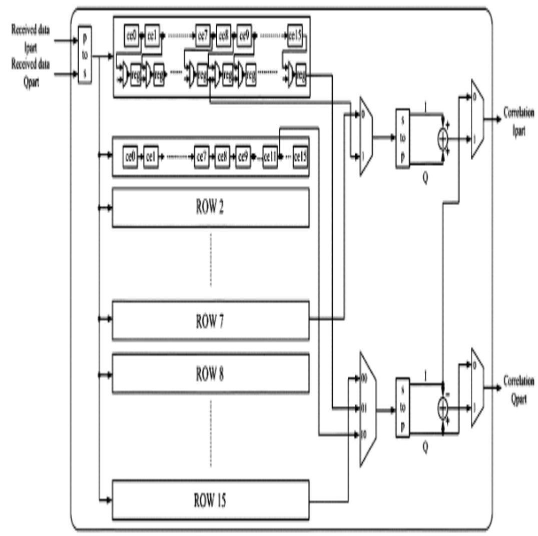

Fig. 5. CE array.

2) MagnitudeCalculation

The CE array outputs the correlation results of the I-channel and the Q-channel. Thus, a non coherent combination of two parts for the purpose of magnitude calculation is needed.

3) Accumulation

In the WCDMA stage 1, accumulation over 15 slots is necessary to increase its SNR. Temporary accumulation results are stored in SRAM since the number of uncertainty is up to 2560.

4) Peak Detector

The peak detector compares and finds the maximum value which can identify the timing information (i.e., slot boundary in WCDMA stage 1, frame boundary in CDMA2000, and SYNC field boundary of 802.11 g) or the transmitted SSC in WCDMA stage 2 and the transmitted scrambling code in WCDMA stage 3.

5) CFRS Decoder

The CFRS decoder is designed to decode comma-free Reed–Solomon code in WCDMA stage2.

6) Ballot

After the 256 chips correlation of the WCDMA stage 3, a ballot machine is needed to vote the most possible scrambling code. The length of the scrambling code is

38 400 chips. Thus, we have to vote 150 times at most to decide which scrambling code the transmitter transmits.

V. LOW POWER DESIGN

In synchronizer most power consumption occurs in CE array. Adders play an important role when calculating the CE's .So applying low power techniques in the design of the adders to improve the power dissipation of the synchronizer Techniques: 1.A spurious power suppression technique (SPST) 2. Absolute weighted magnitude 3. Power management. Fig. 6 illustrates a spurious power suppression technique (SPST) adder in which it is further divided into most significant part (MSP) and least significant part (LSP) sub adders to reduce adder operations. This SPST adder is especially effective for PN-code synchronizations since it mostly results in very small values. Moreover, in order to calculate the true magnitude of signals, multiplications or squares, such as $y=a^2+b^2$ are usually required in non coherent combiners. In the synchronizer, however, peak values of signals are enough when searching cells.

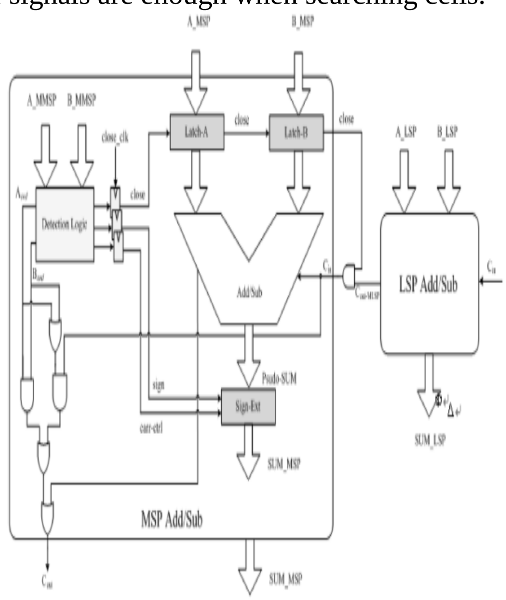

Fig .6 SPST adder

The peak value could be found through comparing the magnitude values of signals. An approximation of the squares can be used to reduce the hardware complexity, and hence the power dissipation. The magnitudes of signals are then transferred to the peak detector. Furthermore, there are a total of 256 CEs, but they are not activated in each application. In this design, an additional power-management mechanism is included to gate the data flow in the CE, as well as the clock in the CE rows. Fig.6 shows the enable mechanism in each CE row. Data can be kept out of the CE rows to avoid unnecessary operations. The global clock for the CE rows is gated to reduce the power dissipation in the registers.

VI. CONCLUSION

In this paper we designed an ASIC which integrates the code synchronization of WCDMA, CDMA2000, and 802.11 g systems. There are three low-power techniques applied in this ASIC design, and proved power consumption can be reduced 57.37% in WCDMA synchronization, 6.06% in CDMA2000 synchronization, and 84.69% in 802.11 g synchronization.

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