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An Phase-Locked Loop Frequency Synthesizer with Minimal Lock-in Time for Continuous-Time Sigma-Delta Analog

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ABSTRACT
Phase-locked loop (PLL) circuit employing a Phase Frequency Detector with NOR gates and a divide-by-64 pseudo-NMOS divide-by-2 frequency divider. This design, intended for a Continuous-Time Sigma-Delta ADC operating at a 640MHz frequency, is meticulously developed and simulated in TSMC 0.18um 1P6M CMOS process technology. The objective is to minimize chip area and achieve a rapid lock-in time. The PLL design demonstrates a fast lock time of approximately 2.5 microseconds, a crucial factor for the ADC clock generator's lock-in time. The desired output frequency of 640MHz is achieved across all corners, ranging from 608MHz to 672MHz, staying within the 640MHz ±5% tolerance. The proposed design employs a charge pump current of 77uA, well within the typical range of charge pump current values (10uA to 100uA).In terms of chip core area, the PLL design exhibits minimal values of 8.3393 nm² and 0.2049 μm² for off-chip and on-chip filters, respectively. This PLL configuration holds significance for its application in ICs utilized in electronic and communication devices, where clock rates and timing relationships are of utmost importance.

Keywords: *phase-locked loop (PLL)*

1.Introduction

The paper also discusses the broader context of PLLs in digital systems, emphasizing the necessity for clock synchronization in binary data processing. Traditional clock references, such as quartz crystal oscillators, have limitations in providing the higher frequencies demanded by modern processing technologies. PLLs emerge as a solution to generate well-timed clocks for high-performance digital systems, ensuring reliable synchronization even as clock frequencies rapidly increase.As a solution to the challenge of generating a 640MHz frequency needed for a continuous-time sigma-delta ADC, the paper proposes the use of a PLL with a stable 10MHz crystal reference frequency. The design aims to minimize chip area and achieve a fast lock-in time, considering the increasing data rates and processing demands in contemporary digital systems.

Different architectural choices are explored and compared, with the selected sub-circuits integrated into the overall PLL design. Proper floor planning is implemented to ensure the achievement of a minimal chip area.

2.System Design Architecture

As shown in Figure 1, the phase frequency detector (PFD), charge pump (CP), loop filter, voltage-controlled oscillator (VCO), and divide-by-64 frequency divider make up the main parts of the system architecture of the planned 640 MHz phase-locked loop (PLL). The phase difference between the feedback clock and the reference clock is used by the phase frequency detector, which functions as a comparator to provide an erroneous output signal. Small frequency variations over time cause a phase mistake to build up. The PFD sends synchronized "up" or "down" signals to the charge pump/low-pass filter when there is a phase difference. The charge pump is prompted by a "up" signal to apply charge to the low-pass filter capacitor, which raises the control voltage (Vcontrol). On the other hand, a "down" signal causes the low-pass filter capacitor to lose charge, which lowers Vcontrol. The VCO receives its input from Vcontrol. The low-pass filter is necessary to store the charge from the charge pump and arantees that only DC signals reach the VCO.

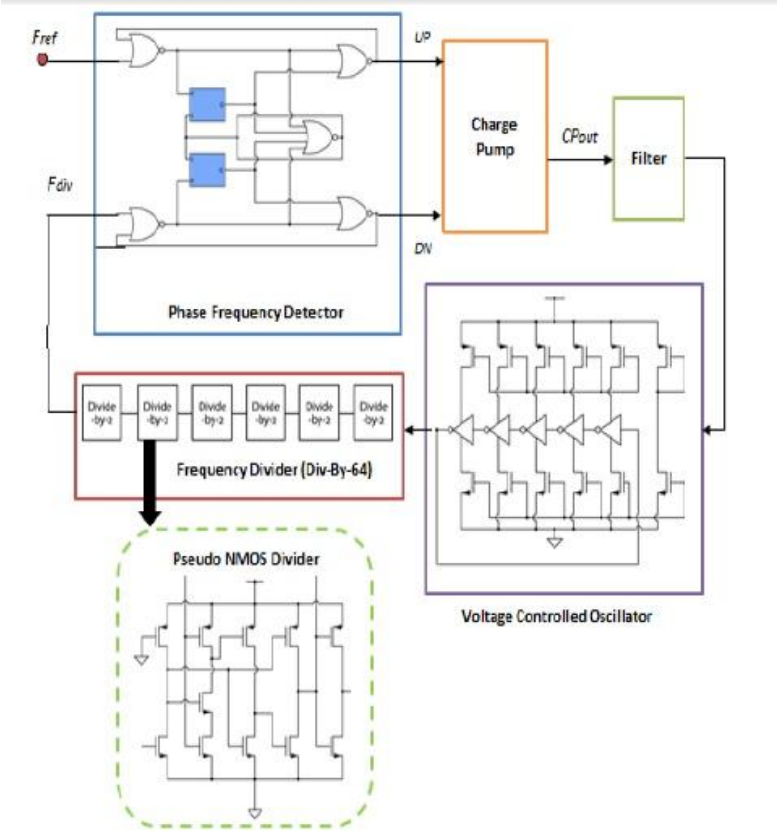

Figure 1. PLL System

In response to the phase frequency detector's (PFD) error signal, the voltage-controlled oscillator's (VCO) job is to modulate the feedback signal's speed. When the PFD sends a "up" signal, the VCO speeds up, and when it sends a "down" signal, the VCO slows down. Next, a frequency divider is used to divide the oscillation frequency such that it is in sync with the feedback clock. Achieving phase locking requires the feedback clock to match the same frequency while maintaining a consistent phase error.

Producing evenly spaced up (up) and down (dn) pulses is the primary function of the Phase Frequency Detector (PFD) [2]. Included as a reset mechanism to guarantee a minimum pulse width at the PFD output, even in the absence of phase error, a four-input NOR gate is used to minimize the potential dead zone [5]. The dead zone, caused by the interaction between the switching time of the charge pump currents and the propagation delay of the internal gates for PFD reset, is eliminated by using the NOR gate [6]. Here, the phase frequency detector makes use of NOR gates to identify the phase difference between the reference crystal oscillator's two inputs.

3. PFD

In response to the Phase Frequency Detector's (PFD) output error signal, the charge pump—the second part of the Phase-Locked Loop (PLL)—acts. To charge or discharge the loop filter capacitor, the charge pump (CP) produces current pulses in reaction to the signal from the PFD [7]. Two logic inputs control the charge pump's two switched current sources, which in turn direct current into or out of the loop filter.

Figure 3 shows three possible states of the circuit. In the first, with QA=0 and QB=0, the output voltage is kept constant because both switches are off. The capacitor is charged by the current flowing via the PMOS branch when QA=1 and QB=0. If, on the other hand, QA=0 and QB=1, the capacitor is discharged by the current flowing through the PMOS branch. Maintaining a constant charge/discharge current regardless of the charge pump's output voltage is a crucial component of any efficient charge pump [1]. The goal is accomplished by making sure that the currents flowing through the PMOS and NMOS branches are roughly equal.

The charge pump's current source is designed according to the current equation given in (1). To make sure the charge pump works and to avoid current mismatch, the transistors are sized carefully.

4.Charge Pump

A voltage-controlled oscillator (VCO) is an electronic oscillator crafted to have its oscillation frequency regulated by a voltage input. In the context of a Phase-Locked Loop (PLL), the oscillation frequency of the VCO is controlled by the charge pump voltage.

Among the various VCO circuit types, the current-starved voltage-controlled oscillator is widely utilized, particularly in integrated circuit (IC) design due to its simplicity compared to LC oscillators that involve inductors.

After evaluating different VCO circuit options, a ring VCO design was selected for this PLL, leveraging its advantages for achieving a minimum chip area. The chosen circuit comprises 5 stages, with an odd number of stages being crucial for oscillation. It is noteworthy that the number of stages must be odd to ensure proper oscillation.

For the frequency divider in this project, a pseudo-NMOS logic design is employed instead of the TSPC divider. The TSPC divider and conventional static logic are unsuitable for frequency division since the input to the divider is a sinusoidal signal from the VCO. Figure 5 depicts the cascaded divide-by-2 frequency divider. To achieve the desired frequency division of 64, six cascaded divide-by-2 frequency dividers are employed (2n=64, where n=6).

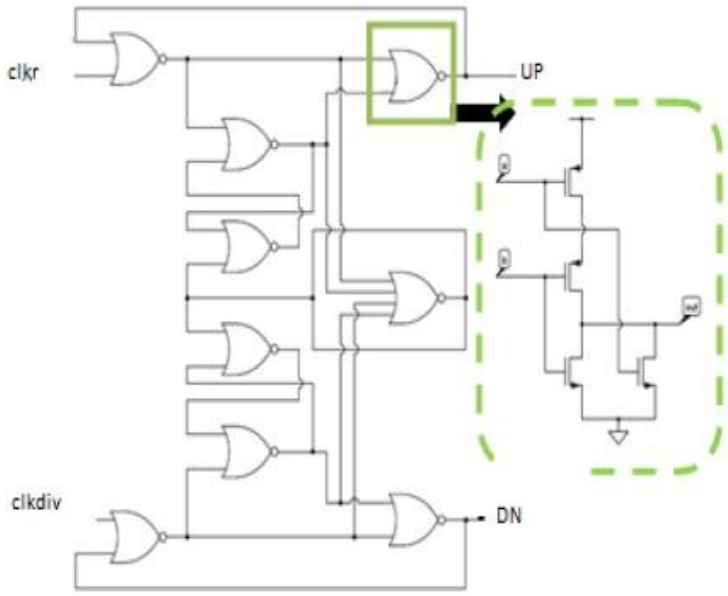

Figure 2. Charge Pump

5. Simulation Results

The Designer tool in conjunction with the TSMC 0.18um CMOS technology process. Before the design could be considered complete, every component had to pass its own set of tests and encounter its own set of problems. A.Simulation of the System and Blocks When clkref is ahead of clkdiv, the charge pump's response is to increase the voltage input to the Voltage-Controlled Oscillator (VCO), as shown in Figure 6, and when clkref is behind clkdiv, the charge pump's response is to decrease the voltage input. suggested Phase-Locked Loop (PLL) architecture was modeled and implemented using the Synopsys Custom.

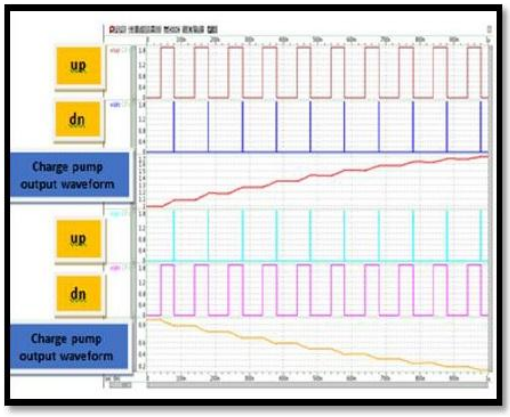

Figure 3: Charge Pump Simulation

6. Performance Analysis

In terms of performance comparison, the proposed research demonstrates superiority in two key parameters: lock-in time and chip area. The fast lock-in time of the proposed Phase-Locked Loop (PLL) is particularly advantageous, given the high clock rates exceeding 10Msps in modern high-speed Analog-to-Digital Converters (ADCs). For a fast-locking PLL, an acceptable lock-in time is typically around 3.78us [15]. This research achieves a lock time of approximately 2.5us, which falls within the acceptable range for the lock-in time of the ADC clock generator. However, excessively fast clocks with settling times in the nanoseconds range are not desirable, as they may introduce more spurs and noise into the dynamics of the PLL.Regarding chip area, the proposed PLL design adheres to the minimum rule, emphasizing efficiency and compactness in its implementation.

7. Conclusion

Using a 640 MHz clock frequency and TSMC 0.18um 1P6M CMOS technology process, this study finishes the design of a 10-MHz reference input Phase Locked Loop that is suited for Continuous-Time Sigma-Delta ADCs. With a lock-in time of 2.5 us, the necessary output frequency of 640 MHz is reached on all corners and is within 640 ± 5%. In order to address the issue of phase error detection, the design of the phase frequency detector resulted in a tiny dead zone, which improved accuracy. By utilizing a pass-gate circuit, the designers of the single-ended charge pump were able to achieve a small current mismatch and minimal skew between the up' and down (dn) inputs. The design of the divide-by-64 frequency divider took great attention in sizing the W/L of each MOS in order to avoid loading effects and delays.

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