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Current Commutated Soft-Switching Converters with Low High Mediations

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Abstract— Zero-current commutation (ZCC) and natural voltage clamping (NVC) eliminate the need for active-clamp circuits or passive snubbers required to absorb surge voltage in conventional current-fed topologies. Switching losses are reduced significantly owing to zero-current switching of primary-side devices and zero-voltage switching of secondary-side devices. Turn-on switching transition loss of primary devices is also negligible. Soft switching and NVC are inherent and load independent. The voltage across primary-side device is independent of duty cycle with varying input voltage and output power and clamped at rather low reflected output voltage enabling the use of low-voltage semiconductor devices. These merits make the converter good candidate for interfacing low-voltage dc bus with high-voltage dc bus for higher current applications. Steady state, analysis, design, simulation, and experimental results are presented.

IndexTerms **—** Zero Current Commutation (ZCC), Natural Voltage Clamping (NVC), Snubbers,Topology, Soft Switching, Simulation.

I. INTRODUCTION

Transport electrification has received significant interest owing to limited supply of fossil fuels and concern of global climate change. Battery-based electric vehicles (EVs) and fuel cell vehicles (FCVs) are emerging as viable solutions for transportation electrification with lower emission, better vehicle performance, and higher fuel economy. Compared with pure battery-based EVs, FCVs are quite appealing with the merits of zero-emission, satisfied driving range, short refueling time, high efficiency, and high reliability. A diagram of a typical FCV propulsion system is shown in Fig. 1.

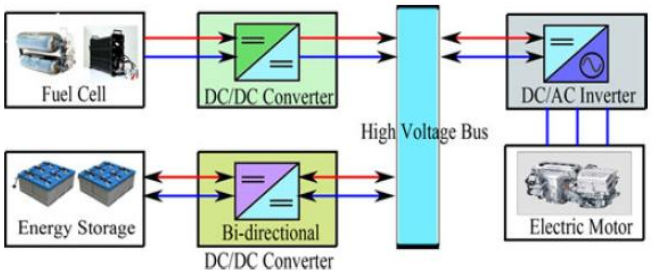

Fig.1 FCV Propulsion System

Bidirectional and unidirectional dc/dc converters are utilized to develop high-voltage bus for the inverter. The energy storage system (ESS) is used to overcome the limitations of lacking energy storage capability and fast power transient of FCVs. Bidirectional converter with high boost ratio and high efficiency is required to connect the low-voltage ESS and high-voltage dc-link bus. Compared with non-isolated topologies, high-frequency (HF) transformer isolated converters are preferred with merits of high step up ratio, galvanic isolation, and flexibility of system configuration. HF transformer isolated converters could be either voltage-fed or current fed. Advantages and disadvantages of both types are compared.

The voltage-fed converters have low switch voltage ratings enabling the use of switches with low ON-state resistance. This can significantly reduce conduction loss of primary-side switches. However, voltage-fed converters suffer from several limitations, i.e., high pulsating current at input, limited soft-switching range, rectifier diode ringing, duty cycle loss (if inductive output filter), high circulating current through devices and magnetic, and relatively low efficiency for high-voltage amplification and high-input current applications.

Compared with voltage-fed converters, current-fed converters exhibit smaller input current ripple, lower diode voltage rating, lower transformer turns-ratio, negligible diode ringing, no duty cycle loss, and easier current control ability. Besides, current-fed converters can precisely control the charging and discharging current of ESS, which helps achieving higher charging/discharging efficiency. Thus, current-fed converter is more feasible for the application of ESS in FCVs. Three topologies of isolated current-fed dc/dc converters, i.e., full-bridge, L-type half-bridge, and push–pull have been researched. One drawback of current fed converters is the high turn-off voltage spike across the devices. Normally, active-clamp circuits, RCD passive snubbers, or energy recovery snubber are employed to absorb the surge voltage and assist soft-switching. In RCD snubbers, energy absorbed by the clamping capacitor is dissipated in the resistor resulting in low efficiency. Active clamp suffers from high current stress (peak) and higher circulating current at light load.

A. Leakage Inductance And Parasitic Capacitance

The leakage inductance and parasitic capacitance of the HF transformer were utilized to achieve zero-current switching (ZCS). However, resonant current is much higher than input current that increases the current stress of devices and magnetic requiring higher VA rating components. Besides, the variable frequency modulation makes the control implementation difficult and complex. External auxiliary circuits are utilized to achieve ZCS and reduce the circulating current but complex. Although the trapped energy can be recycled, the auxiliary circuits still contribute to a significant

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amount of loss. In current-fed bidirectional converter, active soft commutation technique is proposed to divert the switch current to another switch through transformer to achieve natural or zero-current commutation (ZCC) thus reducing or eliminating the need of snubber.

B. Novel Secondary Modulation

In this system, a novel secondary modulation-based naturally clamped soft-switching bidirectional snubberless current-fed push–pull converter is proposed as shown in Fig. 2. Natural voltage clamping (NVC) with ZCS of primary devices is achieved by proposed secondary modulation and therefore avoids the need of passive snubbers or active clamp making it snubberless. Switching losses are reduced significantly owing to ZCS of primary switches and ZVS of secondary switches that permits HF switching operation with smaller magnetic. The objectives of this paper are to explain steady-state operation and analysis, illustrate design, and demonstrate experimental performance of the proposed converter.

C. Operation And Analysis Of The Converter

For the sake of simplicity, the following assumptions are made to study the operation and explain the analysis of the converter: 1) Boost inductor L is large enough to maintain constant current through it. 2) All the components are ideal. 3) Series inductors Llk1 and Llk2 include the leakage inductances of the transformer. The total value of Llk1 and Llk2 is represented as Llk T. Llk represents the equivalent series inductor reflected to the high-voltage side. 4) Magnetizing inductance of the transformer is infinitely large.

II. BOOST MODE OPERATION

In this part, the steady-state operation and analysis with ZCC and NVC concept has been explained. Before turning OFF one of primary-side switches (say S1), the other switch (say S2) is turned-on. Reflected output voltage 2Vo/n appears across the transformer primary. It diverts the current from one switch to the other one through transformer causing current through just triggered switch to rise and the current through conducting switch to fall to zero naturally resulting in ZCC. Later, the body diode across switch starts conducting and its gating signal is removed leading to ZCS turn-off of the device. Commutated device capacitance starts charging with NVC.

The steady-state operating waveforms of boost mode are shown in Fig. 3. The primary switches S1 and S2 are operated with identical gating signals phase-shifted with each other by 180◦ with an overlap. The overlap varies with the duty cycle, and the duty cycle should be kept above 50%. The steady-state operation of the converter during different intervals in a one half HF cycle is explained using the equivalent circuits shown in Fig. 4. For the rest half cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle.

In this interval, primary side switches S2 and anti-parallel body diodes D3 and D6 of secondary-side H-bridge switches are conducting. Power is transferred to the load through HF transformer. The non-conducting secondary devices S4 and S5 are blocking output voltage Vo and the non-conducting primary devices S1 are blocking reflected output voltage 2Vo/n.

Interval 2; $t1 < t < t2$): At $t = t1$, primary switch S1 is turned-on. The corresponding snubber capacitor C1 discharges in a very short period of time. Interval 3; $t2 < t < t3$): All two primary switches are conducting. Reflected output voltages appear across inductors Llk1 and Llk2, diverting/transferring the current through switch S2 to S1. It causes current through previously conducting device S2 to reduce linearly. It also results in conduction of switch S1 with zero current which helps reducing associated turn-on loss.

At the end of this interval $t = t3$, the antiparallel body diode D3 and D6 are conducting. Therefore, S3 and S6 can be gated on for ZVS turn-on. At the end of this interval, D3 and D6 commutates naturally. Current through all primary devices reaches Iin/2. Final values are: ilk1 = ilk2 = Iin/2, iS1 = iS2 = Iin/2, iD3 = iD6 = 0. Interval 4 (Fig. 4(d); $t3 < t < t4$): In this interval, secondary H-bridge devices S3 and S6 are turned-on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 3.

At the end of this interval, the primary device S2 commutates naturally with ZCC and the respective current iS2 reaches zero obtaining ZCS. The full current, i.e., input current is taken over by other device S1. Final values are: ilk1 = iS1 = Iin, ilk2 = iS2 = 0, iS3 = iS6 = Iin/n. Interval 5 (Fig. 4(e); $t4 < t < t5$): In this interval, the leakage inductance current ilk1 increases further with the same slope and anti-parallel body diode D2 starts conducting causing extended zero voltage to appear across commutated switch S2 to ensure ZCS turn-off. Now, the secondary devices S3 and S6 are turned off. At the end of this interval, current through switch S1 reaches its peak value. This interval should be very short to limit the peak current though the transformer and switch reducing the current stress and kVA ratings.

Interval 6 (Fig. 4(f); $t5 < t < t6$): During this interval, secondary switches S3 and S6 are turned-off. Antiparallel body diodes of switches S4 and S5 take over the current immediately. Therefore, the voltage across the transformer primary reverses polarity. The current through the switch S1 and body diodes D2 also start decreasing.

At the end of this interval, current throughD2 reduces to zero and is commutated naturally. Current through S1 reaches Iin. Final values: ilk1 = iS1 = Iin, ilk2 = iD2 = 0, iD4 = iD5 = Iin/n. Interval 7 (Fig. 4(g); $t6 < t < t7$): In this interval, snubber capacitor C2 charges to 2Vo/n in a short period of time. Switch S2 is in forward blocking mode now. Interval 8 (Fig. 4(h); $t7 < t < t8$): In this interval, currents throughS1 and transformer are constant at input current Iin. Current through antiparallel body diodes of the secondary switches D4 and D5 is at Iin/n.

The final values are: ilk1 = iS1 = Iin, ilk2 = iS2 = 0, iD4 = iD5 = Iin/n. Voltage across the switch S2VS2 = 2Vo/n. In this

half HF cycle, current has transferred from switch S2 to S1, and the transformer current has reversed its polarity.

III. Buck Mode Operation

In the reverse direction, the converter acts as a standard voltage-fed full-bridge center-tapped converter with inductive output filter. The regenerative braking energy can be fed back and recharge the low-voltage storage from high-voltage bus, thus increasing overall system efficiency. Standard phase-shift PWM control technique is employed to achieve ZVS of high-voltage side and ZCS of low-voltage side. At low-voltage side, devices need not be controlled because body diodes of the devices can take over as high-frequency rectifier.

The steady-state operating waveforms of buck mode are shown in Fig. 5. The secondary-side diagonal switch pairs S3–S6 and S4–S5 operated with identical gating signals phase shifted with each other by 180◦ with a well-defined dead time gap. The steady-state operation of the converter during different intervals in a one half HF cycle is explained using the equivalent circuits shown in Fig. 6. Interval 1 (Fig. 6(a); to < t < t1): In this interval, secondary side switch pair S3–S6 and body diode D2 of primary-side switch are conducting. Power is transferred to the battery from high-voltage dc-link bus through HF transformer. The values of current through various components are: iD1 = 0, iD2 = ibattery, iS3 = iS6 = ilk = ibattery/n. Voltage across the diode D1: VD1 = 2Vo/n. Voltage across the switches S4 and S5: VS4 = VS5 = Vo. Interval 2 (see Fig. 6(b); t1 < t < t2): At t = t1, secondary side switch pair S3–S6 is turned-off. ilk charges the snubber capacitor C3 and C6 and discharges the snubber capacitor C4 and C5 in a short period of time. Simultaneously, the capacitor C1 discharges very fast. At the end of this interval t = t2, the body diode D4 and D5 are conducting. As long as the Hbridge devices S4 and S5 are turned ON before ilk changes its direction, ZVS turn-on can be assured. Final values are: iD4 = iD5 = ilk = ibattery/n, iD1 = 0, iD2 = ibattery, VD1 = 0; VS4 = VS5 = 0, VS3 = VS6 = Vo.

Interval 4 (Fig. 6(d); t3 < t < t4): In this interval, S4 and S5 are turned-on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 3. At the end of this interval, current flowing through body diode D2 decreases to zero obtaining ZCS. Final values are: ilk = −ibattery/n, iD1 = ibattery, iD2 = 0.

IV. Architectural Design

PWM – Pulse Width Modulation

OVBM – Optimal Voltage Balancing Method

In this system we use Stacked Multicell Converters (SMC) with 2 separate points, each one provides unique voltages and inputting it to the step up converters, which automatically boost up the value of the cells and return the boosted output voltage. The two different cell output voltages are gathered at a point and make the summation of these voltages; we can get

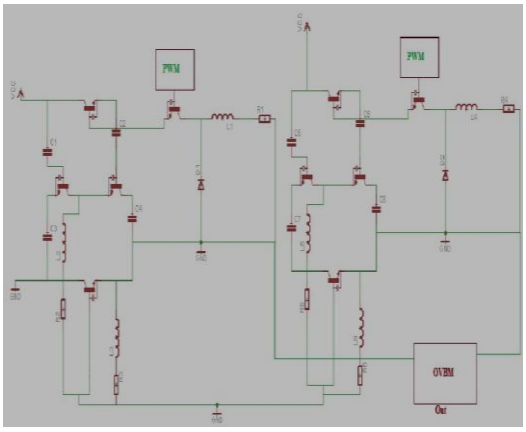

Fig.2 Circuit Diagram

the higher voltage level as a result. Again the equalizer is used to optimize the voltage to get the resulting level more accurately.

V. Simulation and Experimental Results

Proposed converter has been simulated using software PSIM 9.0.4. Simulation results for input voltage Vin = 12 V, output voltage Vo =300 V, output power Po =250W, device switching frequency fs = 100 kHz are illustrated in Fig. 8. Simulation results coincide closely with theoretically predicted waveforms. It verifies the steady-state operation and analysis of the converter presented. Waveforms of current through the input inductor L and voltage.

The ripple frequency of input inductor current iL is 2× fs resulting in a reduction in size. Voltage waveform VAB shows that voltage across the primary switches is naturally clamped at low voltage, i.e., 2Vo/n. Fig. 8(b) shows current waveforms through primary switches S1 and S2 and secondary switches S3 and S4 including the currents flowing through their respective body diodes, phase shifted with each other by 180◦ (S1 versus S2, S5 versus S6). Primary switch currents [I (S1), I (S2)] are diverted from one switch (say S1) to the other one (S2) causing one switch to rise to Iin and the other one to fall to zero.

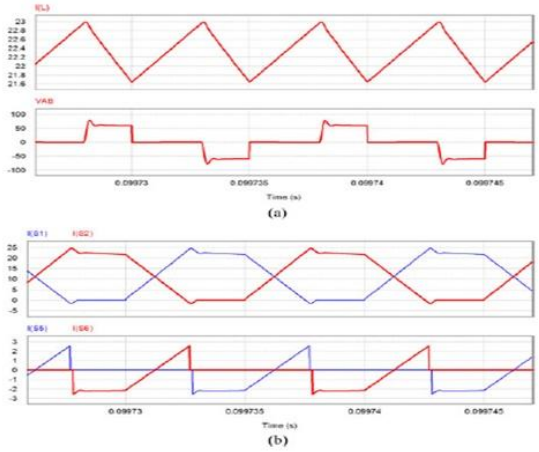

Fig.3 Simulation Results for Output Power of 250w at 300v. (a) Current through Input Inductor I_L and Voltage V_{AB}. (b) Primary

Switches currents i_{s1} and i_{s2} and Secondary switches currents i_{s3} and i_{s4}

This clearly demonstrates claimed ZCC of primary switches. The negative primary currents correspond to conduction of body diodes before the switches are turned-off, which ensures ZCS turn-off of the primary switches. As shown in current waveforms of S3 and S4 in Fig. 8, the antiparallel diodes of switches conduct prior to the conduction of corresponding switches, which verifies ZVS of the secondary-side switches.

Experimental prototype of the proposed push–pull converter, as shown in Fig. 9, is built for the specifications and design given in Section III. Details of the experimental converter are given in Table II. Since the total value of leakage inductance of HF transformer is lower than the desired value given, two external small size series inductors have been added, which can be avoided in practical industrial converter if transformer is designed properly. Also, slight deviation in this value should not affect the performance too much. Gate signals are generated using Xilinx Spartan-6 FPGA design platform.

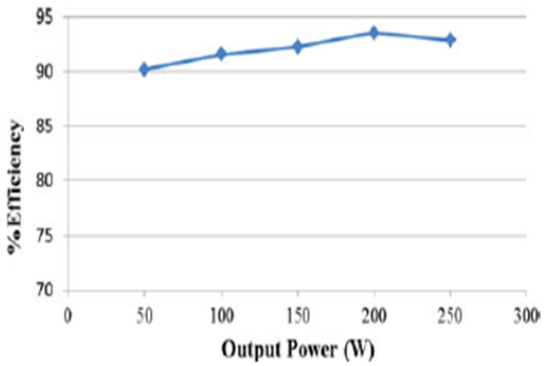

Fig.4 Plot of Efficiency versus Output Power for Different Load Distribution

Experimental results for output power of 250 and 100 W at 300Vare shown in Figs. 8 and 9 respectively. Parts (c) and (d) of Figs. 8–9 show gate-to-source Vgs and drain-to-source Vds voltage waveforms across the primary devices, and the device current waveform. This clearly confirms the ZCS of primary devices. Current through the switch naturally goes to zero and antiparallel body diode starts conducting prior to removal of gate signal. It can be clearly noticed from the waveforms that gate voltage Vgs falls to zero and thereafter, the switch voltage Vds starts rising.

VI. CONCLUSION

This system presents a novel soft-switching snubberless bidirectional current-fed isolated push–pull dc/dc converter for application of the ESS in FCVs. A novel secondary-side modulation method is proposed to eliminate the problem of voltage spike across the semiconductor devices at turn-off. The above claimed ZCC and NVC of primary devices without any snubber are demonstrated and confirmed by the simulation and experimental results. ZCS of primary-side devices and ZVS of secondary-side devices are achieved, which reduces the switching losses significantly. Soft-switching is inherent and is maintained independent of load. Once ZCC, NVC, and soft switching are designed to be obtained at rated power, it is guaranteed to happen at reduced load unlike voltage-fed converters. Turn-on switching transition loss of primary devices is also shown to be negligible. Hence, maintaining soft switching of all devices substantially reduces the switching loss and allows higher switching frequency operation for the converter to achieve a more compact and higher power density system. Proposed secondary modulation achieves natural commutation of primary devices and clamps the voltage across them at low voltage (reflected output voltage) independent of the duty cycle. It, therefore, eliminates requirement of active-clamp or passive snubber. Usage of low voltage devices results in low conduction losses in primary devices, which is significant due to higher currents on primary side. The proposed modulation method is simple and easy to implement. These merits make the converter promising for interfacing low-voltage dc bus with high-voltage dc bus for higher current applications such as FCVs, front-end dc/dc power conversion for renewable (fuel cells/PV) inverters, UPS, microgrid, V2G, and energy storage. The specifications are taken for FCV but the proposed modulation, design, and the demonstrated results are suitable for any general application of current-fed converter (high step-up). Similar merits and performance will be achieved.

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