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# Elimination Of Leakage Current in Tranformer-less CMI Based PV System

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***Abstract—*** In the renewable energy sources, PV system forms the reliable for power generation. Thus the transformerless CMI is considered to be the best alternative for low cost and high efficiency photovoltaic systems. Eliminating the leakage current is one of the most important issues for transformerless inverters in grid-connected photovoltaic system applications, where the technical challenge is how to keep the system common-mode voltage constant to reduce the leakage current. However due to the result of leakage current resulted from the parasitic capacitance efficiency and reliability is reduced. The leakage current caused due to common mode and differential mode voltage is also reduced in this paper is also analysed.So the problem due to transformerless PV inverter should be tackled carefully. In this paper the basic H –bridge is replaced by QZSI because it offers low impedance to high frequency harmonics. The QZSI circuit differs from that of a conventional ZSI in the LC impedance network interface between the source and inverters. Thus filter based suppression solution is used to reduce the leakage current. Thus analysis and solution for elimination of leakage current is done and verified using simulation tool MATLAB and result is obtained.

***Keywords—*** CMI – cascaded multilevel inverter, leakage current ($i_{lesk}$), PV-photovoltaic, THD-total harmonic distortion, qZSI-quasi z source inverter ,CM-common mode, DM-differential mode, $C_{CM}$ – CM capacitor ,Cpv – PV parasitic capacitor, PCC-point of common coupling.

## I. INTRODUCTION

Energy resources and their utilization will be a prominent issue of this century, the problems of natural resource depletion, environmental impacts, and the rising demand for energy resources have been discussed frequently in recent years. Several forms of renewable energy resources, including wind, solar, bio, geothermal, and so forth have gained more prominence and are being researched by many scientist and engineers .solar cell installation involve the use of multiple solar panels or modules ,which can be connected in series or in parallel to provide the desired voltage level to the inverter.

The cascaded H-bridge multilevel inverter topology requires a separate dc source for each H-bridge so that high power and high voltage that from the combination of multilevel modules in a multilevel inverter would favor this topology. To maximize the energy harvested from each string, a maximum power point tracking strategy is needed. The cascaded structure can also generate high quality output waveforms with each semi conductor device switching at low frequency.

The CMI based PV system found its application in both utility-scale and commercial/residential PV systems. It is to be noticed that in previous cases galvanic connection is provided between DC and bulk power AC transmission system using high frequency transformer. But it results in reduced efficiency due to losses in extra components and also results in high cost. Hence, transformerless CMI is preferred for residential/commercial application with low PCC voltage because of low cost and high efficiency. It can be accomplished by extending number of cascaded module.

However the removal transformer results in galvanic connections among grid and the separate PV panel/string interfaced with different cascaded inverters. Due to the parasitic capacitance between the PV panel and the earth results in leakage current, circulates leakage currents can flow through the panels and ground, leading to increased output harmonic content, higher losses, safety and electromagnetic interference. Hence various techniques are dealt to reduce the leakage current.

The leakage suppression techniques for transformerless string inverter have been well established. They can be categorized into three different groups as modulation solution, topology solution and filter solution. The bipolar modulation topologies strategy can significantly reduce the leakage current by maintaining constant common mode voltage but output current quality is degraded and conversion efficiency is decreased. The full bridge topology need extra dc or ac switches, are develop to address the leakage current issue. The above two solution cannot be directly adopted in CMI to tackle the leakage current problem owing to the unique circulating current loops found among the cascaded modules. The filter solution is to bypass loop of which impedance is very low for high frequency common mode noise, thereby preventing the leakage current from flowing outside.

The high amplitude inverter bus MHZ voltage ringing over to semiconductor device is the main concern in the above papers, while the ground leakage current has not been discussed. For paralleled converters, circulating current are generated due to asynchronous switching operations. In such kind of systems, since there is no capacitance involved in circulating current loop, most high frequency can be mitigated by interphase inductor and hence low frequency circulating

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current has to be dealt. This paper identifies the leakage current path in CMI based PV and reduces the leakage current by adding properly passive filter in the inverter with reduced number of switches at high switching frequency. Simulation and experimental results are providing to validate the results of the proposed solution.

## II. Analysis Of Leakage Current And Parasitic Capacitance

The transformerless CMI can be built using basic H-Bridge inverter or modified ones such as Z-source inverter/quasi Z-source inverter mainly for wide range input voltage. Because the Z source/quasi Z source network offers low impedance paths for low frequency noises and leakage current issues. The phase leg voltage sources are named as $v_{ia}$ and $v_{ib}$,i=1,2,…,n are pulse width modulated voltages which are composed of dc components, fundamental frequency components, baseband harmonics, carrier harmonics and its sideband harmonics. The carrier harmonics and its sideband harmonics are the main contributors to the leakage current issue whose magnitude depends on the inverter input voltages and modulation strategy.

Due to parasitic capacitance and several grounding points, multiple circulating leakage current loop are formed in the CMI can be divided into two different types. The first kind is formed by the parasitic capacitor, Inverter Bridge, line inductor and grid ground named as module line leakage current loop. The other kind is formed among inverter bridges; it is indicated as intermodule leakage current. It is a capacitive coupling path with negligible inductance, so high frequency PWM voltages would generate pulse wise leakage current in the loop. The intermodule leakage current loop is a unique loop exists in the PV CMI and it cannot be eliminated even if there is a transformer at the total output of cascaded inverter. Several modified inverter topologies and modulation strategies are proposed to maintain the CM output to be constant to solve the leakage current.

But it does not solve the intermodule circulating loops. To solve the extra intermodule circulating loops, the leakage currents are no longer determined by maintaining CM voltage constant instead DM output voltage also should contribute. The above mentioned modulation or topology cannot be directly implemented to solve the leakage current issue in CMI.The common mode voltage and differential mode voltage is define as $v_{dmi}=v_{ia}-v_{ib}$ and $v_{cmi}= (v_{ia}+v_{ib})/2$ respectively. The filter based two suppression solution is designed at different allocation to reduce the intermodule leakage current and available for different application.

## III. Leakage Current Suppression Solution

The basic structure is compared with proposed structure that CM capacitor ($C_{cm}$), ac-side and dc-side chokes ($L_{cm\text{-}ac}$ and $L_{cm\text{-}dc}$) are added in each inverter module. The voltage and current across parasitic capacitance ($C_{pvi}$) are denoted as $V_{cpvi}$ and $i_{leak}$ respectively. In this paper the $L_{cm\text{-}ac}$ and $L_{cm\text{-}dc}$ merged into the same position so that it would have the same contribution on the leakage current suppression on the system. About the leakage current, the German standard VDE-0126 1-1 defines a leakage current limit (peak value) equal to 300mA. If current is greater than this value the system may be disconnected within 0.3s.

It has been demonstrated that varying common-mode voltage is the primary cause of the leakage current, hence the waveforms of the common mode voltage VPE across the coupling capacitor to ground CPE allows predicting the leakage current exceeding. They also identify the electromagnetic interference noises and eliminate using ac-side and dc-side EMI filter. By the combination of ac-side and dc –side filter, it would compensate on added cost and size. The switches required are also reduced in this paper, hence, switching losses and cost is also reduced. The total harmonic distortion is also reduced gives the added advantage.

The quasi z-source inverter (QZSI) is a single stage power converter derived from the Z-source inverter topology, employing a unique impedance network. The conventional VSI and CSI suffer from the limitation that triggering two switches in the same leg or phase leads to a source short and in addition, the maximum obtainable output voltage cannot exceed the dc input, since they are buck converters and can produce a voltage lower than the dc input voltage. Both Z-source inverters and quasi-Z-source inverters overcome these drawbacks; by utilizing several shoot-through zero states. A zero state is produced when the upper three or lower three switches are fired simultaneously to boost the output voltage. Sustaining the six permissible active switching states of a VSI, the zero states can be partially or completely replaced by the shoot through states depending upon the voltage boost requirement

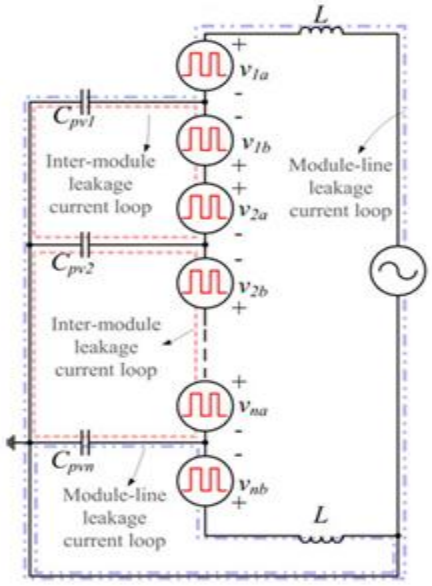



Fig (1) Equivalent Circuit for CMI based PV system

## IV. SIMPLIFIED ANALYSIS AND FILTER DESIGN

The filter based suppression solution for leakage current reduction can be expressed analytically and derived based on the equivalent circuit model. The inverter is model is selected and expressed as follows $z_i$=j ($L_{cm-dc+}$ $L_{cm-ac}$)+1/( jω($C_{pvi}$+ 2$C_{cm}$),i=1, 2,…,n and $Z_L$=jωL.According to the superposition principle the branch current through the inductance of $x^{th}$ inverter is calculated as follows:

$I_{zx}=\sum_{i=1}^{1}$ $(v_{i1}/Z_{si}).Z_{pi}/(Z_x+Z_{pi})$ + $\sum_{i=2}^{x}$ $((v_{ia}-v_{(i-1)b})/Z_{si}).Z_{pi}/(Z_x+Z_{pi})+\sum_{i=x}^{n-1}((v_{ib}v_{(i+1)a})/Z_{si}).Z_{pi}/(Z_x+Z_{pi})+\sum_{i=n}^{n}(v_{nb}/Z_{si}).Z_{pi}/(Z_x+Z_{pi})$…… (1)

Where $Z_{si}$ and $Z_{pi}$ is the impedance in series and parallel with applied voltage respectively. Since the phase leg voltage contains dc components, fundamental –frequency components and baseband harmonics, carrier harmonics and its sideband harmonics. The fundamental frequency leakage current, whose amplitude is relatively small I estimated by shorting the inductors in the circuit due to their low impedances. The frequencies of the carrier harmonics are usually much smaller than the impedance of the designed rated impedance as follows:

$I_{zx}=\sum_{i=1}^{x-1}(v_{ia}-v_{ib})+\sum_{i=x+1}^{n}(v_{ib}-v_{ia})$ $+(v_{xa}+v_{xb})/(2(z_x+z_L)$……..(2)

According to the analytical model the filter is designed to drop the high frequency harmonics across $C_{pvx}$ are lessened. The requirement is fulfilled by designing the resonant frequency circuit lower than the carrier harmonics. The resistance is ignored in the design much smaller than the inductance since it increases the total impedance.

The value of $C_{pvx}$ is mainly depends on the weather condition and hence $C_{cm}$ is added to the circuit which is limited by safety requirement so that resonant frequency filter cannot be designed low. Otherwise, large CM is required and this solution is more suitable for high switching frequency. This constraint depends on the filter size and cost. The figure (2) below shows the circuit diagram for the qzsi network designed with reduced number of switches and filter components.

The suppression CM filters are designed by calculating the leakage currents based on the above equation, the calculated values of leakage current in bridge and ground with different values of ac and dc side chokes and parasitic capacitance value is chosen as 2.2 nF.The RMS value of ground leakage current slightly decreases with increased parasitic capacitance because the impedance of LC circuit increased at the frequencies of the carrier harmonics. According to specific standards the leakage current is greater than the 300 mA or the residual current exceeds to 30mA.in order to limit the leakage current below the standard requirement with safety margin value is 8mH of $L_{cm-dc}$+$L_{cm-ac}$ is used. The majority of carrier frequency voltage harmonics are imposed on the CM chokes, the magnetic design should consider the saturation issue caused by volt-second excitation. The selection of core and core shaped material should fulfill the requirement as follows:

$N_c.A_c=hVS_{max}/B_{sat}$…….. (3)

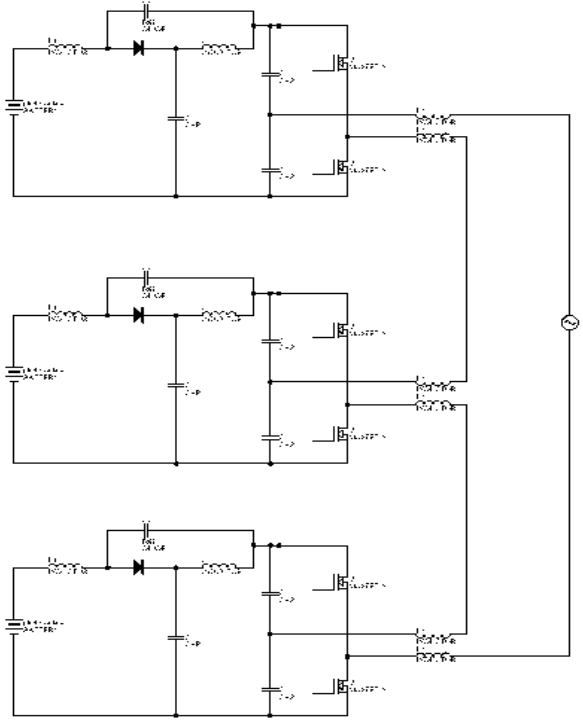


Fig 2: Circuit diagram for CMI based PV system

## V. SIMULATION RESULTS

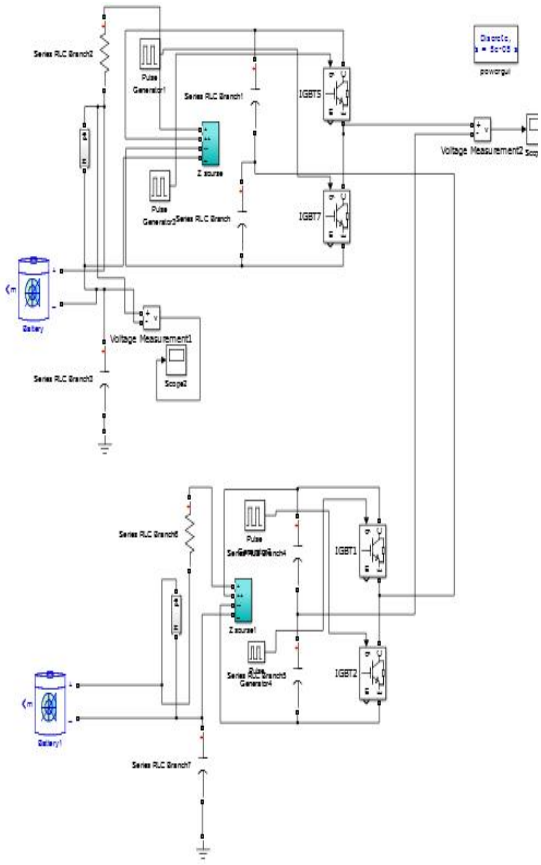
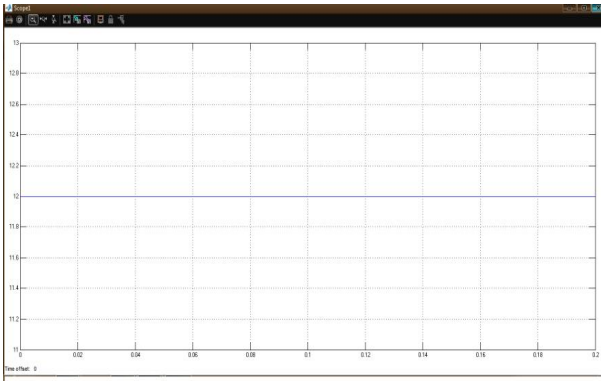
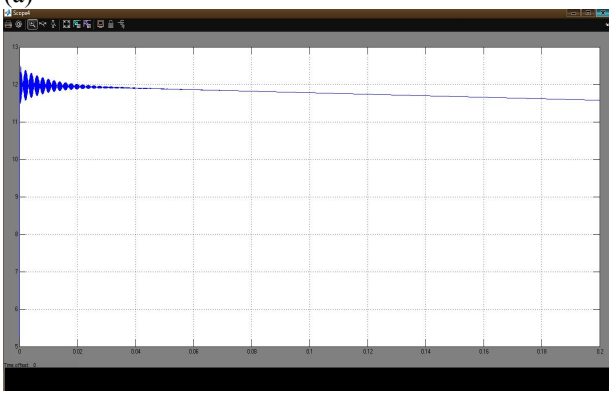


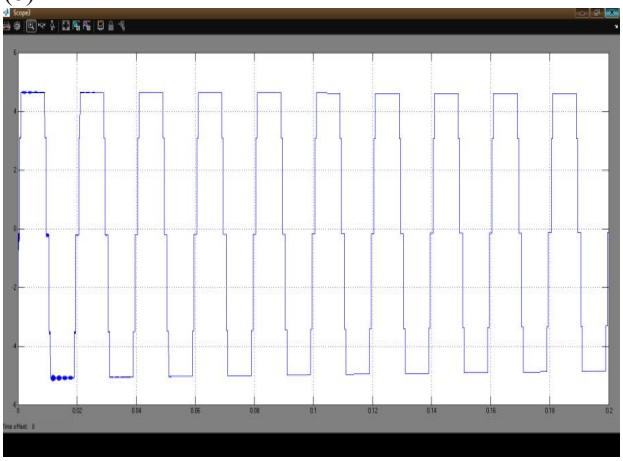
Fig 3: Simulink diagram



(a)



(b)



(c)

(d)

Fig 4 :(a) Input voltage ,(b) Rectified output (c) Leakage current reduction ,(d) Output voltage.

## VI. CONCULSION

This paper presented the analysis of the leakage current occurrence in CMI based PV system caused by the removal of transformer. This leakage current issue features the intermodule leakage current loop among the cascaded inverter module. This leakage current is reduced using filter based suppression solution by constructing LC filter at circulating current paths. The modified H-bridge such as quasi z source network is used for attenuating high frequency noises. The analytical method was used to reduce leakage current issue by utilizing the low capacitance, CM capacitor and parasitic capacitor for high switching frequency.

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