

High Speed Adders using Multi Output Domino Logic

J.Abdulrahumaan , G.Durga

Abstract— Adders are the speed limiting elements to make faster VLSI processors. Carry Look Ahead Adder (CLA) improves the speed by reducing the amount of time required to determine carry bits. The Manchester Carry Chain (MCC) is the most commonly used CLA adder architecture with regular, fast, and simple Domino Logic. Conventional MCC suffers from larger delay during carry propagation. The previous stage of the carry is the main issue which is enhanced in the modified MCC. The intermediate carries are generated by tapping off nodes in the gate which calculates the most significant carry value. The recursive properties of the carries in MCC have enabled the development of multi output domino gates, which enhances the speed improvements with respect to single-output gates. The even and odd carries are computed in parallel. In this work, Residue adder, BCD adders are implemented using Modified MCC based CLA. This work aims at the optimization of propagation delay on the multi output domino logic using TANNER EDA,180nm technology.

IndexTerm - Manchester Carry Chain, Carry Look Ahead Adder, Residue Adder, BCD Adder, Multi Output Domino Logic

I. INTRODUCTION

As the demand for higher performance processors grows, there is a continuing need to improve the performance of arithmetic units and to increase their functionality. High-speed adder architectures include the CLA, carry-skip adders, carry-select adders, conditional sum adders, and combinations of these structures. The MCC is the most common dynamic CLA adder architecture with a regular, fast, and simple structure adequate for implementation in VLSI. The dynamic gates have a problem because is not possible to freely cascade them, these limitation overcome with domino logic. High-speed adders based on the CLA principle are remaining dominant, since the carry delay can be improved by calculating each stage in parallel [1].

In this work both conventional MCC based CLA and modified MCC based CLA architectures are analyzed in terms of power and delay. since the computation of carry for odd bits are independent of even bits, so we can compute in parallel way that leads to reduce in delay and power .

J.Abdulrahumaan, PG Scholar, Dept. of ECE, SSN College of Engineering, Chennai- 603110. (Email: abdulrahumaanf@yahoo.in)
G.Durga , Assistant Professor, Dept. of ECE, SSN College of Engineering, Chennai- 603110. (Email: durgag@ssn.edu.in)

The rest of the paper is organized as follows. Section II deals with the architectures for both MCC based CLA and modified MCC based CLA. Section III deals with Design of Residue Adder and BCD adder using modified MCC.

II. CARRY LOOK AHEAD ADDER ARCHITECTURES

A. Conventional Manchester carry chain

A carry look ahead adder improves speed by reducing the amount of time required to determine carry bits. The carry look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits. The CLA solves the problem of delay it takes to propagate the carry, by calculating the carry signal in advance based on the input signal.

The MCC Adder is a chain of pass-transistors that are used to implement the carry chain [1]. MCC architecture mainly consists of carry propagate and carry generate signal blocks. The carry generate signal is implemented in domino logic [2, 3] shown in Fig 1. Since generate signal possess AND operation if both input are maintained at 1, then the output g_i will be maintained at 1 else the output value will be maintained at 0. The propagate signal implemented in domino logic is shown in Fig 2. Since the propagate signal is implemented in XOR operation. if both the inputs are different then output p_i the inputs are different then output p_i will maintain the value 1, else p_i will have value 0.

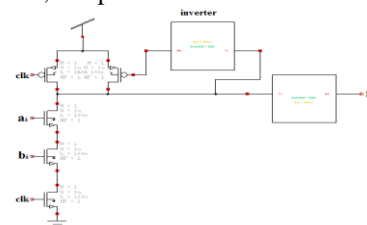


Fig 1. Generate Signal

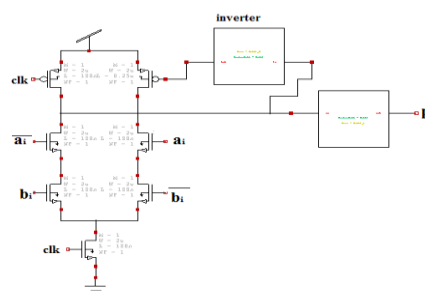


Fig 2. Propagate Signal

In the conventional 4 bit MCC the CLA length is limited to 4 in order to cut down of number of series connected transistors. Fig 3. Shows the conventional implementation of the 4 bit carry chain using multi output domino CMOS logic [4]. This conventional circuit consists of 4 bit two inputs namely p_0, p_1, p_2, p_3 (Propagate signal) and g_0, g_1, g_2, g_3 (Generate signal) respectively.

$$g_i = a_i b_i$$

$$p_i = a_i \oplus b_i$$

$$c_0 = g_0 + p_0 c_{-1}$$

$$c_1 = g_1 + p_1 g_0 + p_0 c_{-1}$$

$$c_2 = g_2 + p_2 (g_1 + p_1) (g_0 + p_0 c_{-1})$$

$$c_3 = g_3 + p_3 (g_2 + p_2) (g_1 + p_1) (g_0 + p_0 c_{-1})$$

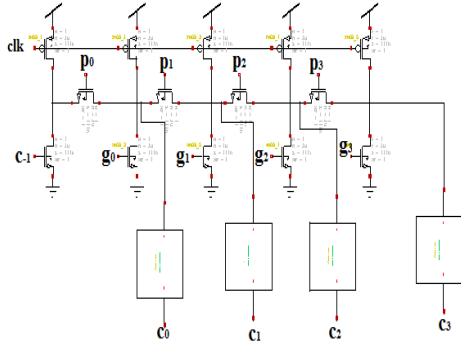


Fig 3. Conventional 4-bit MCC

B. Modified Manchester Carry Chain

A new 8-bit carry chain adder block in multi-output domino CMOS logic is used. The even and odd carries of this adder are computed in parallel by two independent 4-bit carry chains [1]. The New generate signal implemented in domino logic is shown in Fig 4. The new Generate Signal $G_i = g_i + g_{i-1}$ lets g_i is generate signal to perform AND operation, g_{i-1} is previous state of input value g_i . Since generate signal possess operation if both input are maintained at 1, then the output g_i will be maintained at 1 else the output value will be maintained at 0 i.e $G_i = 0$.

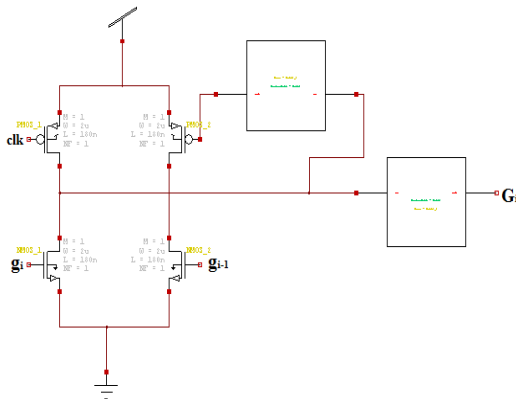


Fig 4. New Generate Signal

The New propagate signal implemented in domino logic is shown in Fig 5. The propagate signal is $P_i = p_i \cdot p_{i-1} \cdot t_{i-2}$ and Fig 6. shows the OR propagated signal.

The new generate and propagate signals G_i and P_i can be easily proven to be mutually exclusive, avoiding false node discharges. These new carry signal is used to compute even carry chain and odd carry chain in parallel. The modified 8-Bit MCC for implementation of wider adders leads to significant operating speed improvement compared to the corresponding adders based on 8-Bit Modified Manchester carry chain using multi-output domino logic.

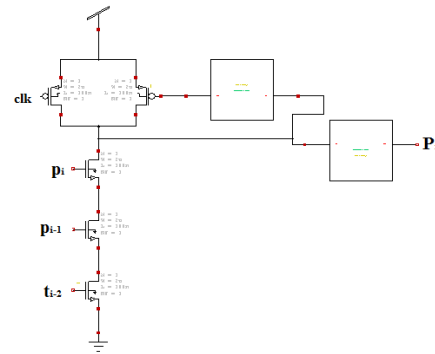


Fig 5. New Propagate Signal

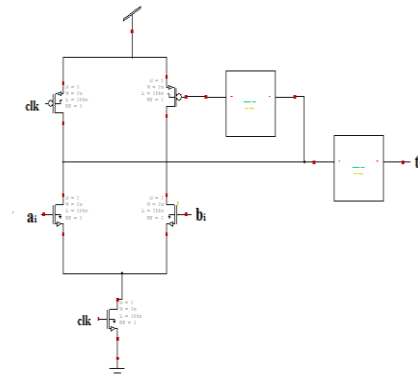


Fig 6. OR Propagate Signal

C. Even Carry Chain

The Even Carry Chain is implemented in multi output domino logic is shown in Fig 7. It consists of 4 bit two inputs namely P_0, P_2, P_4, P_6 (New Propagate signal) and G_0, G_2, G_4, G_6 (New Generate signal) respectively.

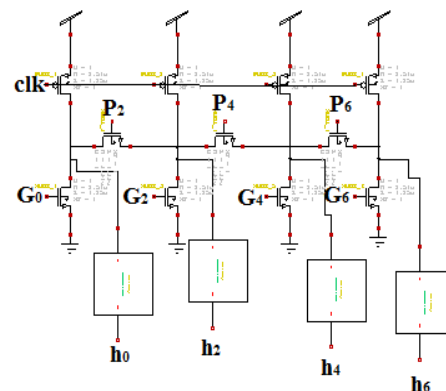


Fig 7. Even Carry Chain

This carry chain gets computed when input value has even values. Say $i = 0, 2, 4, 6$. For the even input values say p_0, p_2, p_4, p_6 and g_0, g_2, g_4, g_6 the corresponding intermediate even carries say h_0, h_2, h_4, h_6 is obtained. The input values of propagate and generate signals are obtained from P_i and G_i respectively. The even carries can be analytically given by

$$\begin{aligned} h_0 &= G_0 c_{-1} \\ h_2 &= G_0 + P_2 G_0 \\ h_4 &= G_4 + P_4 G_2 + P_4 P_2 G_0 \\ h_6 &= G_6 + P_6 G_4 + P_6 P_4 G_2 + P_6 P_4 P_2 G_0 \end{aligned}$$

D. ODD Carry Chain

The ODD Carry Chain is implemented in Multi Output Domino Logic is shown in Fig 8. It consists of 4 bit two inputs namely P_1, P_3, P_5, P_7 (New Propagate signal) and G_1, G_3, G_5, G_7 (New Generate signal) respectively. The operation of the circuit is controlled by clock signal. The input values are get from New P_i and G_i values of the domino propagate and generate output values.

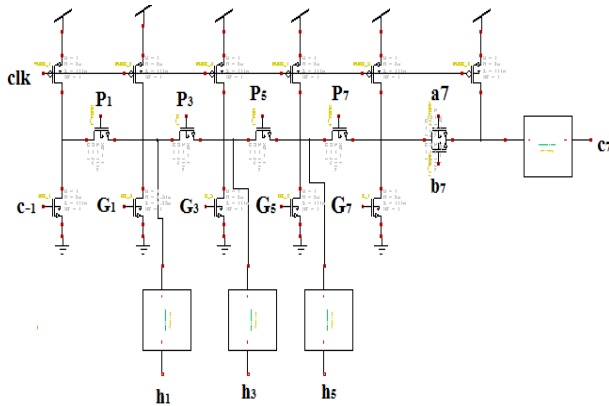


Fig 8. Odd Carry Chain

The input values of propagate and generate signals are obtained from p_i and g_i respectively. The odd carries can be analytically given by

$$\begin{aligned} h_1 &= G_1 + P_1 c_{-1} \\ h_3 &= G_3 + P_3 G_1 + P_3 P_1 c_{-1} \\ h_5 &= G_5 + P_5 G_3 + P_5 P_3 G_1 + P_5 P_3 P_1 G_0 \\ c_7 &= G_7 + P_7 G_5 + P_7 P_5 G_3 + P_7 P_5 P_3 G_1 + P_7 P_5 P_3 P_1 c_{-1} \end{aligned}$$

Fig 9. shows the sum bit implementation using XOR gate, this architecture used in both conventional MCC based CLA and modified MCC based CLA.

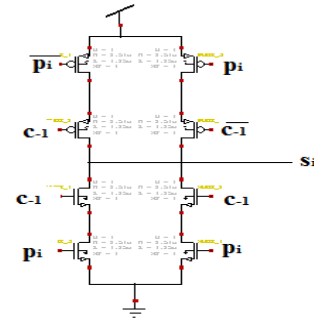


Fig 9. Sum Bit Implementation

To compute sum and carry of even bits on substituting value $a_0 a_2 a_4 a_6$ (0111) and $b_0 b_2 b_4 b_6$ (0001) and input carry c_{-1} is 0 and respective sum $s_0 s_2 s_4 s_6$ (0110) and carry $h_0 h_2 h_4 h_6$ (0001) and the respective output waveform of even bits is shown in Fig 9. To compute sum and carry of odd bits on substituting value $a_1 a_3 a_5 a_7$ (1011) and $b_1 b_3 b_5 b_7$ (1001) and input carry c_{-1} is 0 and respective sum $s_1 s_3 s_5 s_7$ (0110) and carry $h_1 h_3 h_5 c_7$ (1001) and the respective output waveform of even bits is shown in Fig 10.

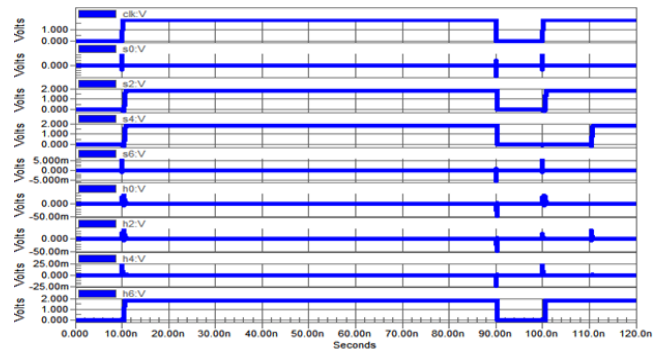


Fig 10. Simulation Waveform for even bits

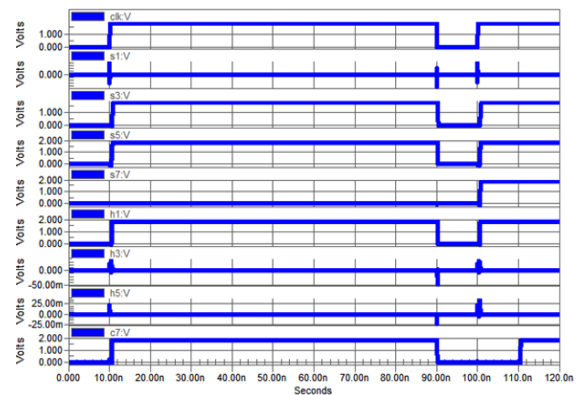


Fig 11. Simulation Waveform for odd bits

III. DESIGN OF RESIDUE ADDER AND BCD ADDER USING MODIFIED MCC

A. Residue Adder

Residue adders are fundamental arithmetic components typically employed in residue number system -based digital signal processing systems. we are proposing a residue adder

based on Modified CLA [1] using domino logic. Residue adder implemented using the carry look ahead (CLA) algorithm which reduces delay due to carry propagation by calculating the carries to each stage in parallel. Bayoumi [5,6] described a modulo adder that utilizes two binary adders and a multiplexer. The first adder adds A and B. the second one adder sum to $2^n - m$ which is nothing but 2's complement of m. The carry bit generated by the first and second adder indicates whether or not $A+B$ is greater than m. If anyone carry out of the two adders is 1 the second adder sum is the result otherwise first adder result is the final result. Instead of conventional adder we used modified MCC based CLA is used shown in Fig 11. To compute sum and carry on substituting value of first adder for even bits $a_0a_2a_4a_6(0100)$ and $b_0b_2b_4b_6(1001)$ and input carry c_{-1} is 0 and respective sum $s_0s_2s_4s_6(1101)$ and carry $h_0h_2h_4h_6(0000)$ and $m=6$ chosen for 2's complement. The second adder input is first adder sum (1101) and 2's complement of m(0101) and respective second adder sum (1010) and carry(0101) and the respective output waveform of residue adder for even bits is shown in Fig 12.

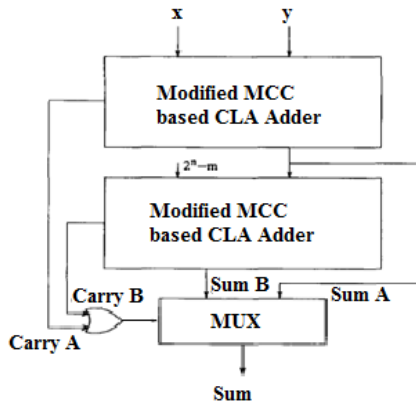


Fig 12. Block Diagram of Residue Adder

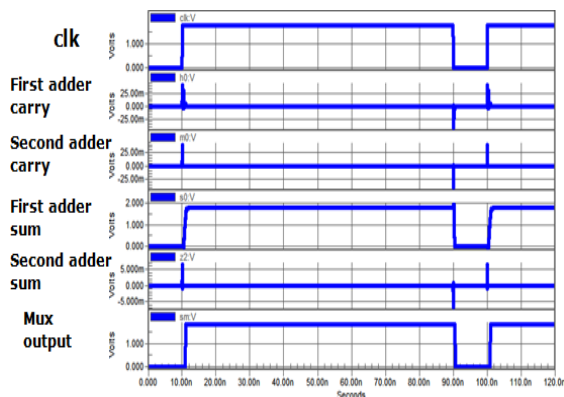


Fig 13. Simulation Waveform of Residue adder for even bits

To compute sum and carry on substituting value of first adder for odd bits $a_1a_3a_5a_7(0100)$ and $b_1b_3b_5b_7(1001)$ and input carry c_{-1} is 0 and respective sum $s_1s_3s_5s_7(0011)$ and carry $h_1h_3h_5h_7(1100)$ and $m=6$ chosen for 2's complement. The second adder input is first adder sum (0011) and 2's complement of m(0101) and second adder sum (0001) and

carry(1111) and the respective output waveform of residue adder for odd bits is shown in Fig 13.

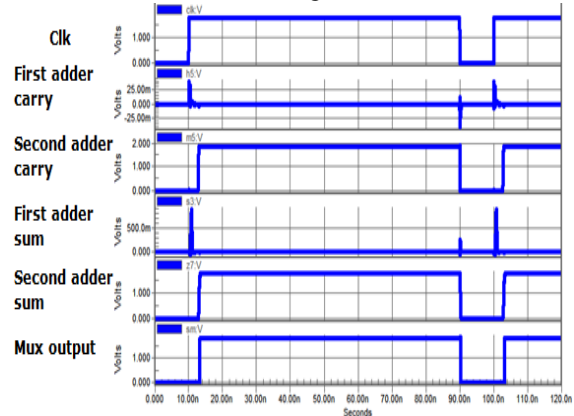


Fig 14. Simulation Waveform of Residue Adder for odd bits

B. BCD Adder

Computers or calculators that perform arithmetic operations directly in the decimal number system represent decimal numbers in binary coded form. An adder for such a computer must employ arithmetic circuits that accept coded decimal numbers and present results in the same code[7,8], variety of possible decimal adder circuits are presented in literature, one of such adder is considered here and also we are replacing normal binary adder with modified MCC based CLA[1]shown in Fig14. BCD adder calculates arithmetic addition of two decimal digits. If the sum is upto 9: use the regular adder, If the sum is >9 : use the regular adder and add 6 to the result[9,10].

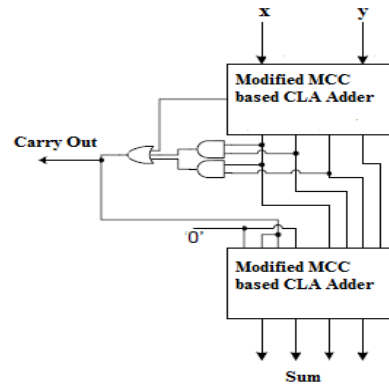


Fig 15. Block Diagram of BCD adder

To compute sum and carry on substituting value of first adder for even bits $a_0a_2a_4a_6(1000)$ and $b_0b_2b_4b_6(0010)$ and input carry c_{-1} is 0 and respective sum $s_0s_2s_4s_6(1010)$ and carry $h_0h_2h_4h_6(0000)$. Here sum is 5(1010) i.e less than 9 so first adder sum is the result and the respective output waveform of BCD Adder for even bits is shown in Fig 15.

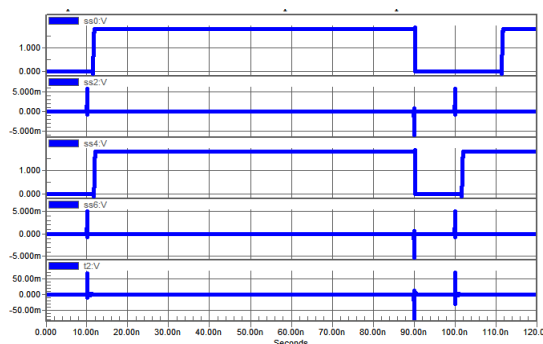


Fig 16. Simulation Waveform of BCD Adder for odd bits

To compute sum and carry on substituting value of first adder for odd bits $a_1a_3a_5a_7(1011)$ and $b_1b_3b_5b_7(0100)$ and input carry c_{-1} is 0 and respective sum $s_1s_3s_5s_7(1101)$ and carry $h_1h_3h_5c_7(0100)$. here sum is 13(1101) i.e greater than 9 so first adder sum with add 6 is the final result and the respective output waveform of BCD Adder for even bits is shown in Fig 16 .

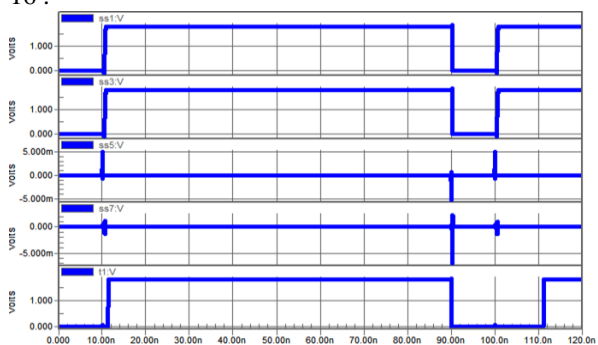


Fig 17. Simulation Waveform of BCD Adder for Odd Bits

IV. RESULTS AND DISCUSSIONS

The two architectures of CLA (conventional MCC and modified MCC), are simulated in Tanner EDA and also performance parameters such as power and delay are listed in table I. The performance analysis of residue adder is listed in table II. The performance analysis of BCD adder is listed in table III.

TABLE I. Performance Analysis of CLA Adder

S.NO	Performance Parameters	8-bit CLA using Conventional MCC	8-bit CLA using Modified MCC
1	Delay(n sec)	10.38	5.43
2	Power(mw)	0.232	0.213

TABLE II. Performance Analysis of Residue Adder

S.NO	Performance Parameters	Residue Adder using Conventional	Residue Adder using Modified 8-

		8-bit CLA	bit CLA
1	Delay(n sec)	1.012	0.562
2	Power(mw)	0.902	0.605

TABLE III. Performance Analysis of BCD Adder

S.NO	Performance Parameters	BCD Adder using Conventional 8-bit CLA	BCD Adder using Modified 8-bit CLA
1	Delay(p sec)	683.20	443.26
2	Power(mw)	0.626	0.414

V. CONCLUSION

The MCC is an efficient and widely accepted design approach to construct CLA adders. The presented new Manchester design style is based on two independent carry chains. This design realizes better improvement in reducing the delay by introducing parallelism concept in carry chains. As a result, the 2 separate carry chains namely odd carry chain and even carry chain work in parallel thus increases speed of operation by reducing the delay considerably compared with Conventional MCC. Hence this 8 bit carry chain is more efficient and can operate at low supply voltages with high speed. Also implementation of residue adder and BCD using conventional MCC and modified MCC are reported, Here also modified MCC based CLA gives reduction of delay. In this way, the speed performance is significantly improved with respect to that of modified MCC topology. Modified Carry look ahead adder, Residue adder and BCD in multi output domino logic, and the simulation results are verified using TANNER EDA,180nm technology.

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