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IMPLEMENTATIONS OF TEST PATTERN DESIGN USING CYCLIC REDUNDANCY CHECK

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Abstract— A new low-power scan-based built-in self test (BIST) technique is proposed based on weighted pseudorandom test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST. During the pseudorandom testing phase, an LP weighted random test pattern generation scheme is proposed by disabling a part of scan chains. During the deterministic BIST phase, the design-for-testability architecture is modified slightly while the linear-feedback shift register is kept short. In this paper, we present a novel secure cell design for implementing the design-for-security infrastructure to prevent leaking the key to an adversary under any circumstances. Our proposed design is resistant to various known attacks at the cost of a very little area overhead. In both the cases, only a small number of scan chains are activated in a single cycle. Sufficient experimental results are presented to demonstrate the performance of the proposed LP BIST approach. This Proposed design will be implemented by Verilog HDL and simulated by Modelsim Tool. The Proposed Montgomery Multiplier is Synthesis by Xilinx and FPGA Spartan 3 XC 3S 200 TQ 144.

Keywords— Cyclic redundancy check, FPGA, low cost, programmable, FPGA, Testing

I. INTRODUCTION

The gap between functional and test power consumption is growing bigger and bigger, with the latter reaching 2X to 5X of the former due to the ever-shrinking functional power and ever-increasing test power . Problems, such as excessive heat that may reduce circuit reliability, formation of hot spots, difficulty in performance verification, reduction of the product yield and lifetime, and so on, have become severe . A fast simulation approach was proposed for low-power (LP) off-chip interconnect design. An important through silicon via (TSV) modeling/simulation technique for LP 3-D stacked IC design . Furthermore, the power dissipation of scan-based built-in self-test (BIST) is much higher than power dissipation in deterministic scan testing due to excessive switching activities caused by random patterns. Therefore, it is essential to propose an effective LP BIST approach. However, many of the previous LP BIST approaches cause fault coverage loss to some extent. Therefore, achieving high fault coverage in an LP BIST scheme is also very important. Weighted pseudorandom testing schemes and methods can effectively improve fault coverage. However, these approaches usually result in much more power consumption due to more frequent transitions at the scan flip flops in many cases. Therefore, we intend to propose an LP scan-based pseudorandom pattern generator (PRPG).

Objective the proposed Designs

1. Implementation of Segmented CRC Design architecture
2. Implementation of non-segmented system CRC Design architecture
3. Implementing Circuit Testing using proposed CRC Design
4. Performance analysis of Testing application

Traditional hardware designs based on the LFSR (Linear Feedback Shift Register) tend to have fixed structure without such flexibility. Fully-adaptable CRC accelerator based on a table-based algorithm is proposed. The table-based algorithm is a flexible method commonly used in software implementations. It has been rarely implemented with the hardware, since it is believed that the operational speed is not enough. A weighted test-enable signal-based pseudorandom test pattern generation scheme. False test fail may be generated, with consequent increase in yield loss. it requires a significant increase in number of test vectors. Its occupied More Power & More Delay.

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II. RELATED WORKS

1)Bit-Swapping LFSR and Scan-Chain Ordering: A Novel Technique for Peak- and Average-Power Reduction in Scan-Based BIST, Abdallatif S. Abu-Issa and Steven F. Quigley, May 2009.

This paper presents a novel low-transition linear feedback shift register (LFSR) that is based on some new observations about the output sequence of a conventional LFSR. The proposed design, called bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1 multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions that occur at the scan-chain input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR.

2)Scan Test Cost and Power Reduction through Systematic Scan Reconfiguration , Ahmad Al-Yamani, Narendra Devta-Prasanna

This paper presents segmented addressable scan (SAS), a test architecture that addresses test data volume, test application time, test power consumption, and tester channel requirements using a hardware overhead of a few gates per scan chain. Using SAS, this paper also presents systematic scan reconfiguration, a test data compression algorithm that is applied to achieve 10× to 40× compression ratios without requiring any information from the automatic-test-pattern-generation tool about the unspecified bits.

3)An Efficient Scan Tree Design for Compact Test Pattern Set, Shibaji Banerjee, Dipanwita Roy Chowdhury

In this paper, to circumvent this problem, a new two-pass hybrid method is proposed to design an efficient scan tree architecture based on approximate compatibility. The method is particularly suitable for a highly compact test set having fewer don't cares and low compatibility. Finally, to reduce the volume of scan-out data, test responses shifted out from the leaf nodes of the scan tree are compacted by a space compactor, which is designed especially for the proposed scan tree architecture. The compactor uses an XOR tree, and its overhead is low. The design thus offers a solution to both test data and response compaction.

4)A BIST Pattern Generator Design for Near-Perfect Fault Coverage, Mitrajit Chatterjee and Dhiraj K. Pradhan

A new design methodology for a pattern generator is proposed, formulated in the context of on-chip BIST. The design methodology is circuit-specific and uses synthesis techniques to design BIST generators. The pattern generator consists of two components: a pseudorandom pattern generator and a combinational logic to map the outputs of the pseudorandom pattern generator. This combinational logic is synthesized to produce a given set of target patterns by mapping the outputs of the pseudorandom pattern generator. It is shown that, for a particular CUT, an area-efficient combinational logic block can be designed/synthesized to achieve 100 (or almost 100) percent single stuck-at fault coverage using a small number of test patterns. This method is significantly different from weighted pattern generation and can guarantee testing of all hard-to-detect faults without expensive test point insertion.

5)Low-Power Programmable PRPG with Test Compression Capabilities, Michał Filipek, Grzegorz Mrugalski

This paper proposes an LP test compression method that allows shaping the test power envelope in a fully predictable, accurate, and flexible fashion by adapting the PRESTO-based logic BIST (LBIST) infrastructure. The proposed hybrid scheme efficiently combines test compression with LBIST, where both techniques can work synergistically to deliver high quality tests.

6)Novel Approach to Reduce Power Droop During Scan Based Logic BIS, M. Omaria D. Rossi F. Fuzzi C. Metra

In this paper, we propose a novel approach to reduce peak power/power droop during test of sequential circuits with scanbased Logic BIST. In particular, our approach reduces the switching

activity of the scan chains between following capture cycles. This is achieved by an original generation and arrangement of test vectors. The proposed approach presents a very low impact on fault coverage and test time, while requiring a very low cost in terms of area overhead.

III. PROPOSED TESTING DESIGN

A new LP weighted pseudorandom test pattern generator using weighted test-enable signals is proposed using a new clock disabling scheme. The design-for testability (DFT) architecture to implement the LP BIST scheme is presented. Our method generates a series of degraded sub circuits. The new LP BIST scheme selects weights for the test-enable signals of all scan chains in each of the degraded sub circuits, which are activated to maximize the testability.

A new LP deterministic BIST scheme is proposed to encode the deterministic test patterns for random pattern- resistant faults. Only a part of flip flops are activated in each cycle of the whole process of deterministic BIST. A new procedure is proposed to select a primitive polynomial and the number of extra variables injected into the linear-feedback shift register (LFSR) that encode all deterministic patterns. The new LP reseeding scheme can cover a number of vectors with fewer care bits, which allows a small part of flip flops to be activated in any clock cycle.

In this brief, the stride-by-5 algorithm is proposed to achieve the optimal utilization of FPGA resources. The pipelining go back algorithm is proposed to solve the padding zeros problem. Two algorithms and a method corresponding to the three requirements are proposed to reduce the resource utilization with guaranteed throughput and programmability. First, the stride by- 5 algorithm is proposed, which can reduce the resource utilization compared with the slicing-by-4 and slicing-by-8 algorithms. Second, the pipelining go back algorithm is proposed to solve the padding zeros problem, which will introduce an O (log2 n) resource utilization. Finally, a hardware internal configuration access port (HWICAP) is used to realize dynamic programmability, and it leads to small and constant resource utilization regardless of the bus width.

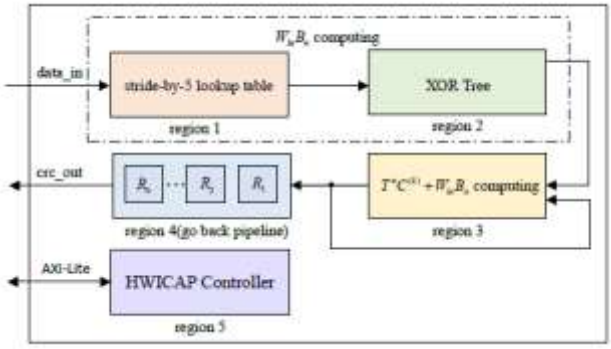


Figure 1 : Non Segmented CRC Design

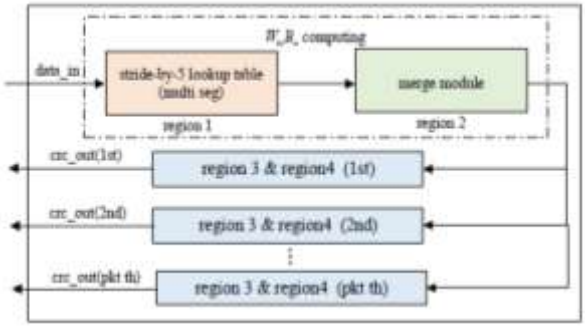


Figure 2 : Segmented CRC Design

A new LP scan-based BIST technique is proposed based on weighted pseudorandom test pattern Generation and reseeding. Proposed Design has multiple advantages listed below. Lower test time area overhead. While requiring a significantly lower test time and comparable area overhead. It does not increase the number of test vectors. It requires a small cost in terms of area overhead.

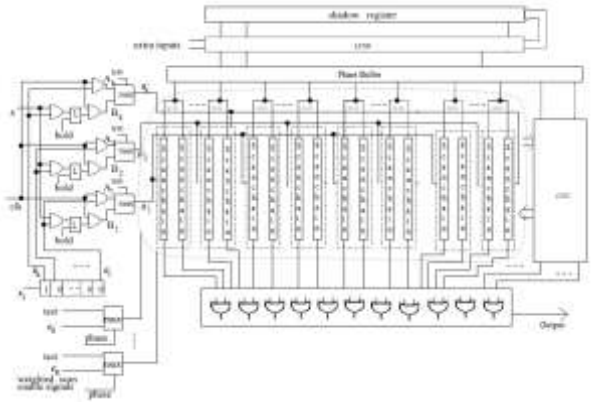
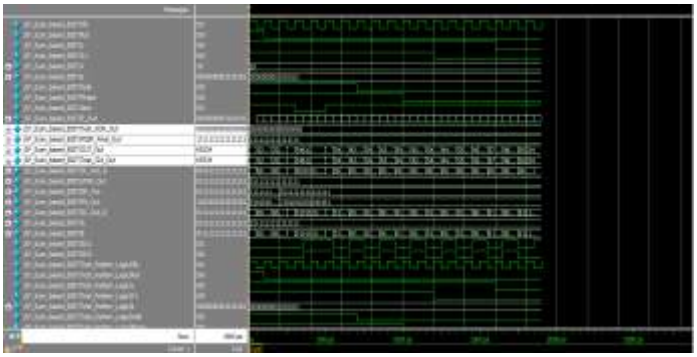


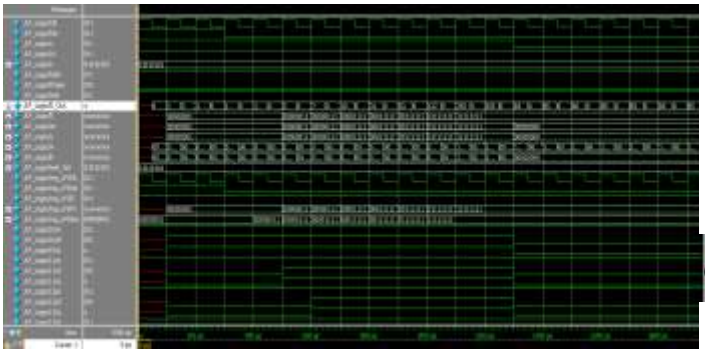
Figure 3. Testing Design

IV. SIMULATION RESULTS

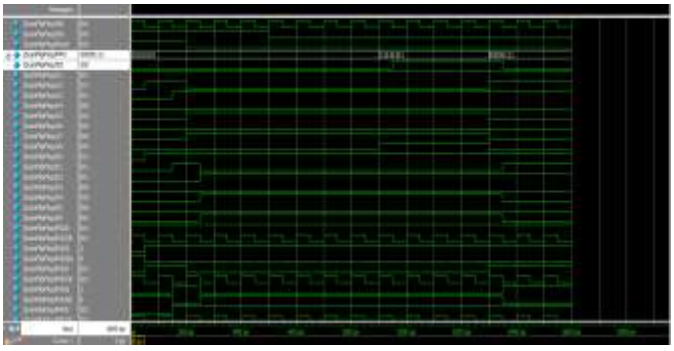
1)LP Scan based BIST



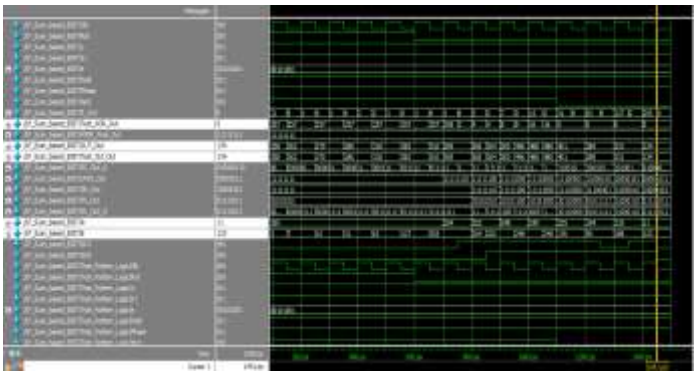
2)LP Logic Code



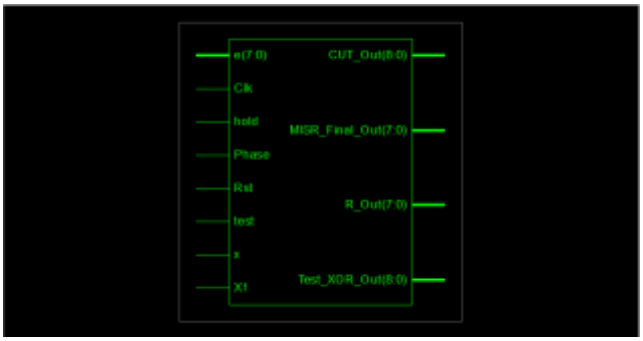
3)Scan Chain New

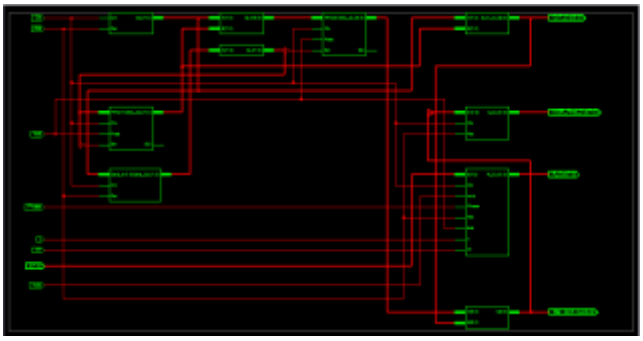


4)LP Scan based BIST without Fault COMBINATIONAL LOGIC

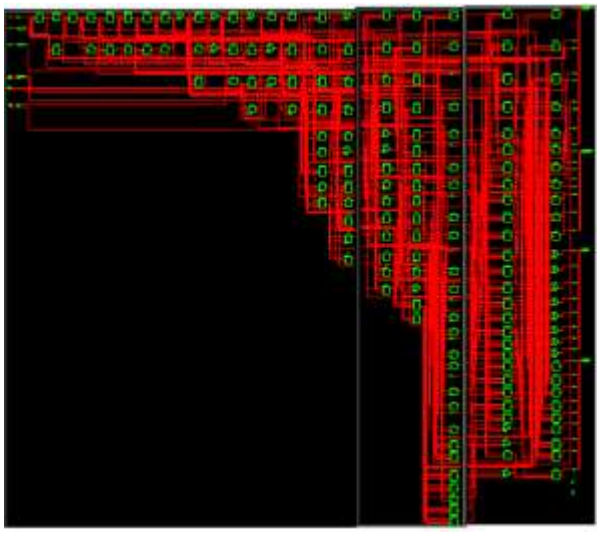


5)RTL View of the proposed Design





6)TECHNOLOGY SCHEMATIC VIEW



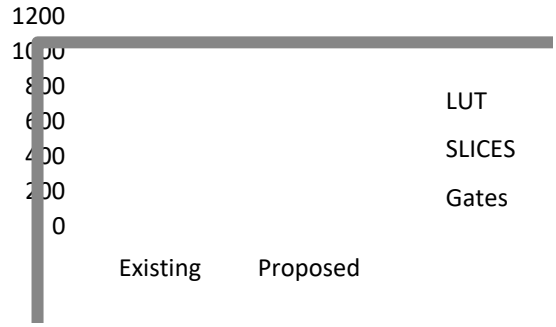
V. COMPARISON AND ANALYSES

The suggested BIST design concepts are built in Verilog HDL, generated with Xilinx for various bit sizes, and the latency and area are compared. As seen in Fig. 4, BIST Design with Segmented and non segmented has the smallest area and has the shortest latency when compare to Conventional BIST as the number of bits increases. The results demonstrate that using proposed design for

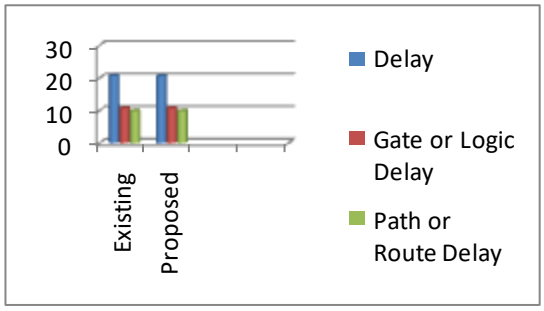
inclusion achieves the suggested Design's overall minimum area.

	Area in Number of LUT			Delay			Power
BIST Design	LUT	Slices	Gate Count	Delay	Gate or Logic Delay	Path or Route Delay	mW
Paper	88	67	1024	20.616ns	10.682ns	9.934ns	338.44
Proposed	80	62	909	20.563ns	10.682ns	9.881ns	225.63

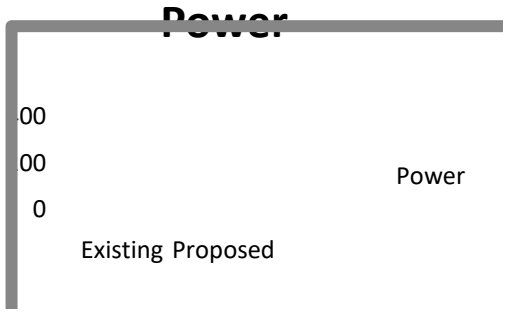
Comparison Chart



Area Analysis



Delay Analysis



Power Analysis

VI. CONCLUSION

A new LP BIST method has been proposed using weighted test-enable signal-based pseudorandom test pattern generation and LP deterministic BIST and reseeding. The new method consists of two separate phases: 1) LP weighted pseudorandom pattern generation and 2) LP deterministic BIST with reseeding. The first phase selects weights for test-enable signals of the scan chains in the activated sub circuits. A new procedure has been proposed to select the primitive polynomial and the number of extra inputs injected at the LFSR. A new LP reseeding scheme, which guarantees LP operations for all clock cycles, has been proposed to further reduce test data kept on-chip. Experimental results have demonstrated the performance of the proposed method by comparison with a recent LP BIST method. The LP reseeding technique is a little more complicated. This work can be extended to latch-on-capture transition fault testing and small delay defect testing.

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