International Journal on Applications in Electrical and Electronics Engineering

Volume 2: Issue 1: January 2016, pp 1-7. www.aetsjournal.com ISSN (Online) : 2395-3527

Improving DC Coverage with Gate Strength Awareness for Small Delay Defect Detection Delay Measurement

H.T. Amarnath
selection grade lecturer,
Electrical and Electronics Engg.
Govt polytechnic chintamani-563125
amarnathht06@gmail.com

S. Nagaraj, selection Grade Lecturer
Electrical and Electronics Engg.
MEI Polytechnic Rajajinagar bengaluru -560010
Kadambha@gmail.com

ABSTRACT

The percentage of systems that met reliability standards dropped significantly from 41% in 1985–1990 to 20% in 1996–2000, as determined by operational tests. The question of testability in different contexts is becoming more pressing as system complexity rises. If we want to keep releasing trustworthy, reasonably priced products to consumers, we must immediately ramp up our efforts to fix testability problems on the device, board, and system levels. The current standard in this field states that 500 DPM is the lowest allowable defect per million. In a matured process, a test coverage requirement of 98% is necessary to reach a 200 DPM target, which usually yields 99%. In order to enhance DC coverage, this work presents a new method—gate strength-aware modeling.

Keywords: Direct current *(DC),* Follow-On Test and Evaluation (FOTE), Developmental Test (DT

1.Introduction

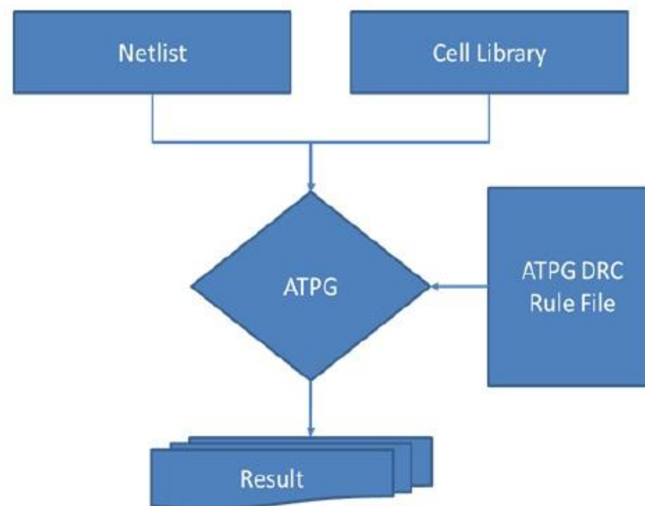
Figure 1 shows that between 1985 and 1990, the percentage of systems passing dependability requirements dropped significantly from 41% to 20% in operational tests. This decline is borne out by the study. Figures 1 and 2 show the relationship between reliability and the Mean Time Between (MTB) for a number of tests and evaluations from 1996 to 2000, including Operating Test II (OT II), Follow-On Test and Evaluation (FOTE), Developmental Test (DT), Operating Test (OT), Limited User Test (LUT), Follow-On Test (FOT), and Initial Operational Test (IOT). The trend keeps getting worse during this time.

Fig. 1 shows that operational reliability against requirements analysis shows that many systems could not achieve the necessary level of dependability, and that this tendency became even more pronounced between 1996 and 2000.

As a result, guaranteeing continuous progress necessitates addressing system testability in every application development effort, and this is true at the device, board, and system levels.

2.DC Coverage Flow

Users can augment the basic scan with N cycles of sequential capture and raise the test abort level in the default Automatic Test Pattern Generator (ATPG) flow for stuck-at-fault testing. Although the ATPG duration is increased, this adjustment is made to improve stuck-at-fault coverage.ThefigureshowsthestandardATPGflow. The default approach to improving test coverage is to collapse fault counts in order to decrease the overall number of faults and the number of fault nodes that cannot be tested, because the ATPG library does not account for the effect of gate drive strength in its models. The Stuck-at-Zero (SA0) causes three faults in an AND gate with a collapsed fault, whereas the Stuck-at-One (SA1) is a dominance fault that can be seen from the gate's output. For an AND gate with two inputs,thesumofallcollapsedfaultsisfour. By reporting collapsed faults, the total fault count is greatly reduced and effective fault coverage is improved. This is because most IP cell counts are buffer, inverter, AND, OR, NAND, and NOR gates. The complete chip collapsed coverage report and the uncollapsed coverage report are compared to show that these improvements are there.



.

Figure 1. ATPG Flow

.

3. Cell Aware Model

The main goal in the context of Mentor's Cell-Aware Automatic Test Pattern Generation (ATPG) modeling [17]-[20] is to improve bridging coverage by means of library modeling that is specific to Mentor's ATPG tool. A demand for a pattern set based on logic in a 3-to-1 input multiplexer (MUX) provides an example of this. As can be seen from the comparison between Tables IV and V, testing a 3-to-1 input MUX requires more patterns to accommodate the greater bridging fault coverage. As an example, the ATPG tool typically reports 12 faults for default 3-to-1 MUX modeling, taking into account that the MUX has 5 input ports and 1 output port. Using cell-aware technology to model the 3-to-1 multiplexer (MUX) allows for improved bridging fault identification in library modeling without changing the library structure. This is demonstrated in Figure 6, which is the capacitive coupling report for bridging tests.

4.Design Concept

New Very Large Scale Integration (VLSI) chips should perform much better as a result of scaling breakthroughs in semiconductor processing technology. But small-delay flaws, caused by resistive-short, resistive-open, or resistive-via difficulties, become more problematic as scaling increases. These flaws, if missed during LSI screening, might cause chips to act abnormally during certain operations in specific applications and shorten their lifespan since transistors age so quickly. Therefore, there needs to be an immediate improvement in the testing quality for small-delay fault identification in order to guarantee reliability post-shipping.

To find and fix small-delay problems, timing delays in circuit routes is essential. Even with a high resolution, external testers are unable to detect delays in very tiny circuit pathways. As a result, methods for measuring embedded delay are highly necessary. The scan-based delay measuring approach, which uses a variable clock generator, is one such methodology. This method steadily reduces the test clock width with high resolution while continually sensitizing the path under inspection in order to evaluate the latency of that path. By directly measuring the time it takes for the linked flip-flop to catch a transition from the measured path to its launch, the scan-based delay measurement technique offers a significant accuracy boost. The measured value is unaffected by process variation when the clock generator is compensated since its fluctuation is exclusively dependent on the clock generator's frequency variation.

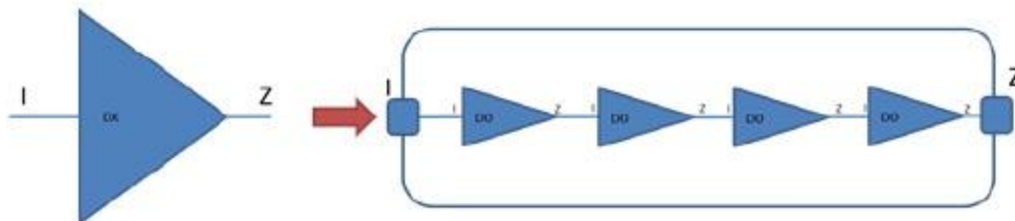


Figure 2. Gate strength ATPG

International Journal on Applications in Electrical and Electronics Engineering
Volume 2: Issue 1: January 2016, pp 1-7. www.aetsjournal.com ISSN (Online) : 2395-3527

Unfortunately, this method isn't viable anymore because it relies on the scan operation time, which is becoming increasingly large compared to the functional clock and scan clock frequencies. Noguchi et al. developed the self-testing scan-FF to solve this problem; it makes measurement time practical by lowering the number of scan operations necessary. On top of that, they suggested a method for the self-testing scan-FF to reduce area. recent approaches still have a large area overhead when compared to traditional scan designs, even with recent improvements. This work presents a signature register-based scan-based delay measurement technique for small-delay defect diagnosis. The expected test vectors are not needed in this procedure because the signature registers examine the test replies. Compared to traditional scan designs for Design for Test (DFT), the overall area cost is equivalent, and the suggested method has a shorter measurement time for delay than traditional scan-based methods.

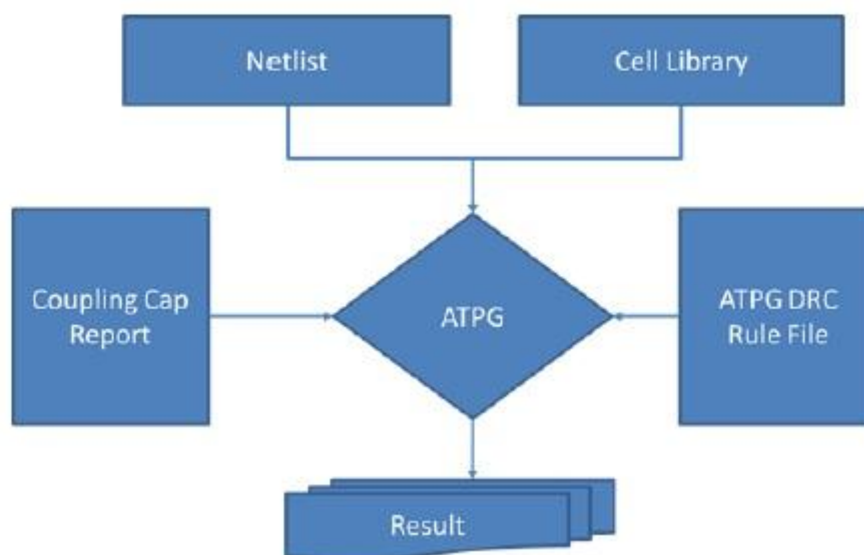


Figure 3. Bridging Test Flow

5. Small Delay Measurement Chip

Presented here is a high-level outline of the suggested measurement approach, complete with descriptions of the ideas, procedures, data volume, area overhead, tester channel reduction method, ATPG constraints, number of extra latches needed, measurement time, and data volume. It also explains how to use transition fault test vectors in response tracing mode to locate the diagnosiswiththelowestfailurefrequency. The primary method for measuring delay in the proposed concept is a scan-based technique, and it is focused on target paths that are sensitive to changes in a single path. The utilization of signature registers and extra latches to speed up the delay measuring process is the main differentiator. In this case, we take the time it takes for a particular path to complete, with the assumption that the clock width is 10 ns while everything is running smoothly and a resolution of 2nswhen measuring delays. The first step of the measurement procedure is to reset the signature register (SIG) to its starting state.

After then, the target path is tested continuously five times, with the test clock being progressively reduced as the resolution increases. You can test different clock widths with the help of the variable clock generator. After every test, the results are delivered to SIG, and after five rounds of delay fault testing, the signature value of SIG is retrieved. By comparing the retrieved signature value with the expected signature values from the signature table, we may estimate the delay.
Measurement cases, test response sequences path delay values, and matching signature values are all part of the signature table. With a resolution of 2 ns, the delay of each path is classified into ranges (greater than 10, 8-10, 6-8, 4-6, 2-4, or 0-2 ns). One way to find the delay value is to compare the retrieved signature value with the predicted values in the database.

Taking into account the target path's clock width (W), measurement resolution (R), number of flip-flops (N), and continuous testing duration (T), the delay measurement sequence is described. Since the test vector is pre-stored in the latches, the suggested approach operates under this assumption.

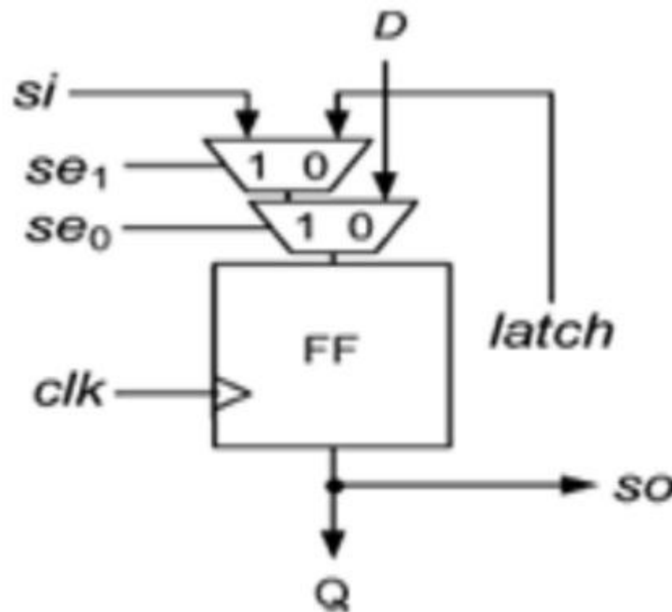


Figure 3: Phase Interpolateor Clock

6. Analysis

The main logic resource for creating synchronous and combinatorial circuits are the Configurable Logic Blocks (CLBs). On each of the four slices that make up a CLB, you'll find two logic-implementation Look-Up Tables (LUTs) and two storage elements that can either flip-flop or latch data.

Both a 16-bit shift register (SRL16) and a 16-by-1 memory (RAM16) configuration are available for the LUTs. To top it all off, the slices have multiplexers and carry logic, which makes it easier to create wide logic and math functions. Utilizing the slice resources within the CLBs, the automatic mapping of general-purpose logic in a design is accomplished. Every single CLB is the same, and the Spartan-3E family's CLBs maintain the same structure as theSpartan-3family. See Figure 6 for an illustration of the CLBs' regular array of rows and columns. The array's density changes as the number of CLB rows and columns changes.

7. Conclusion

Two important suggestions are presented in this study. An approach to measuring delays that makes use of signature analysis and a variable clock generator is presented in the first proposal. This approach works with Field Programmable Gate Arrays (FPGAs) as well as System-on-Chip (SoC) applications. Addressing tiny delay problems has also become a crucial concern in FPGA designs because to the continued trend of significant size reduction in FPGA processes. As a result, FPGAs are a good fit for the proposed strategy. The efficient and economical application of the suggested measurement method in field-programmable gate arrays (FPGAs) is one possible direction for future search. Due to the IR loss caused by higher test clock frequencies, there is a chance of increased measurement errors when testing short routes. Test quality can be adversely affected by this. Therefore, addressing and eliminating measurement errors related to the IR drop is another part of future development.

Reference

[1]. An On-Chip Delay Measurement Technique Using Signature Registers for Small-Delay Defect Detection Kentaroh Katoh, Member, IEEE, Kazuteru Namba, Member, IEEE, and Hideo Ito, Member, IEEE 1063-210/$26.00 © 2011 IEEE

[2]. N. Ahmed and M. Tehranipoor, Nanometer Technology Designs: High-Quality Delay Tests. New York: Springer, 2007.

[3]. K. Noguchi, K. Nose, T. Ono, and M. Mizuno, “A small-delay defectdetection technique for dependable LSIs,” in Proc. IEEE Symp. VLSI Circuits, 2008, pp. 64–65. Institute of Electrical and Electronics Engineers (IEEE), *Journal of Solid-State Circuits*, vol. 41, no. 2, p. 433, February 2006.

[4]. Y. Zorian, “Testing the monster chip,” *IEEE Spectrum*, pp. 54-60, 1999.

[5]. B. I. Dervisoglu and G. E. Stong, “Design for testability: Using scanpath techniques for path-delay test and measurement,” in *Proc Int. Test Conf.*, 1991, pp. 365-374.

[6]. S. Kim, M. Soma, and D. Risbud, “An effective defect-oriented BIST architecture for high-speed phase-locked loops,” in *Proc. VLSI Test Symp.*, 2000, pp. 231-236.

[7]. S. C. Ma, P. Franco, and E. J. Mccluskey, “An experiemental chip to evaluate test techniques experimental results,” in *Proc. Int. Test Conf.*, 1995, pp. 663-672.

[8]. (2008). The Evolution and Future of DFx In Modern ICs. Future Fab. [Online]. Available: www.future-fab.com

[9]. S. M. Kang and Y. Lelibici, *CMOS Digital Integrated Circuits: Analysis and Design*, Addition-McGraw Hill, 2003

[10]. P. C. Maxwell, R. C. Aitken, K. R. Kollitz, and A. C. Brown, “IDDQ and AC scan: The war against unmodeled defects,” in *Proc. Int. Test Conf.*, 1996, pp. 250-258.