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LOW POWER CARRY AGEA ADDER DESIGN USING ADIBATIC LOGICS

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Abstract— This paper proposes a two-phase clocked adiabatic static CMOS logic (2PASCL) method for 16bit carry-look ahead adder. The 2PASCAL circuits working on the principles of adiabatic switching can be used for energy recovery. Adders are important components in applications such as digital signal processor (DSP) architectures and microprocessors. Apart from the basic addition, adders are also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc. A schematic and layout of proposed circuit is implemented in Cadence Virtuoso 6.1.5 using 180nm technology. Further power dissipation comparison is made between 2PASCAL and standard CMOS, it shows a significant power saving

Keywords—*2PASCL adiabatic logic, Carry-Look Ahead Adder, Energy recovery, Power supply, Cadence Virtuoso*

I. INTRODUCTION

In conventional CMOS logic circuits, from 0 to VDD transition of the output node, the total output energy drawn from power supply and stored in capacitive network. Adiabatic logic circuits reduce the energy dissipation during switching process, and utilize this energy by recycling from the load capacitance. For recycling, the adiabatic circuits use the constant current source power supply and for reduce dissipation it uses the trapezoidal or sinusoidal power supply voltage.

The equivalent circuit used to model the conventional CMOS circuits during charging process of the output load capacitance. But here constant voltage source is replaced with the constant current source to charge and discharge the output load capacitance. Hence adiabatic switching technique offers the less energy dissipation in PMOS network and reuses the stored energy in the output load capacitance by reversing the current source. Adiabatic Logic does not abruptly switch from 0 to VDD (and vice versa), but a voltage ramp is used to charge and recover the energy from the output.

The types of logic circuits are

- CMOS INVERTER
- CMOS NAND
- CMOS NOR

The recently reported adiabatic circuits like 2PASCL, GFCAL, CEPAL and QSERL mainly suffer from the following imperfections:

(1) output amplitude degradation
(2) large delay
(3) complex circuit structure

The GFCAL circuit has diodes in the charging and discharging path, voltage drop across the diode due to cut-in voltage ($V\gamma$) causes power dissipation when current flow across it. Also, diode-based logic families suffer from output amplitude degradation. Though GFCAL have very less power dissipation in comparison to other adiabatic logic families but it suffers from very large delay at its output and amplitude degradation. Unlike GFCAL circuit, QSERL circuit has two power clocks with two phases. Due to the hold phases it suffers from floating output which results in lack in robustness. The CEPAL circuit has excellent driving ability and robustness, also its throughput does not depend on the frequency ratio; however, it is not so power efficient in comparison to the others. Also, it has one extra diodes in its charging and discharging path both, which will cause large area and other problems. The 2PASCL circuit design does not have diodes in its charging path, thus current flows only through the transistor during charging which will reduce the drawbacks related to the diode-based circuits. Also, instead of using ramp or sinusoidal power clocks here split-level sinusoidal power clocks are used, which have certain

advantages like reduced delay and power dissipation at the output, higher output amplitude, and so forth. 2PASCL circuit structure is simple and similar to static CMOS circuit in comparison to GFCAL and CEPAL circuits. However, the diode used in the pull up network and diode in the pull-down network to recycle the charge from output node causes power dissipation, which cannot be avoided.

Full adders are used in arithmetic circuits, microprocessors, microcontrollers, and other data processing units. All these essentially require arithmetic operations— most basic of them being binary addition. This binary addition needs to be high performance and low power for the device to be efficient and feasible. Thus, an adder is the fundamental component of a processor. The most critical performance parameter of an adder is its power consumption and its importance is magnified manifold due to its current use in portable devices which have limited power supply. Adiabatic logic circuits reduce this energy dissipation during the switching and recycle the energy lost to the ground and utilize it. Thus, these are also called reversible logic circuits. Adiabatic techniques applied to a full adder reduce the power consumption and reuse the energy available. Adiabatic circuits reduce dissipation by following two key rules: 1. Never turn on a transistor when there is a voltage potential between the source and drain. 2. Never turn off a transistor when current is flowing through it. Full adders can be designed using multiple techniques out of which Ripple Carry Adder (RCA) and Carry Look-ahead Adder (CLA) are considered for comparison based on their power and speed characteristics. An RCA consumes the least power but is the slowest (propagation delay is the most) while the CLA is the fastest but requires more power. So, Adiabatic logic is used in CLA to reduce power consumption of the circuit. Applying Adiabatic to an RCA, though lowers the power dissipation a little, it effectively renders the adder impractical as the already high propagation delay is further increased. Thus, a CLA is designed using the reversible Adiabatic logic which results in the power consumption as well as the propagation delay in a practical and usable range and is preferred over the RCA and the other adders.

MOTIVATION OF THE RESEARCH

The carry-lookahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger-value bits of the adder.

II. OBJECTIVES

1. Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply.
2. Thus, the term adiabatic logic is used in low-power VLSI circuits which implements reversible logic.

This work concludes from the above simulation results and comparisons, efficient charge recovery adiabatic logic dissipates power almost 50% less than the conventional static CMOS logic and 2N-2N-2P adiabatic logic dissipates slightly greater than ECRL and less than CMOS logic

In this paper we have implemented two-phase clocked adiabatic CMOS logic (2PASCL) circuits and observed how it works in different phases of input power clock. The simulation results show that power consumption in the 2PASCAL NOT, NAND, NOR, XOR and 16 bit carry-look ahead adder circuits are considerably less than that in a static CMOS adder.

III. EXISTING WORK

The popular methodology among computational logic elements is binary addition. The ripple carry order is an n-nit adder which has n one-bit full adders. Carry is computed in this method until (n-1) the adder has computed the (n-1) the output, the adder is not complete. The total delay of the logic element is done by the carry chain. Therefore speeding up in carrying chain leads to the speeding up an adder. As the speed of addition with reminds amount of power is the main criteria, carry look ahead adder is chosen, the one way to speed up the carry computation is carry look ahead adder. The carry computation is broken into 2 steps by CLA, starting with the computation of two intermediate values. The adder has 2 inputs ai and bi, then propagate (pi) and generate(gi) is given by

$Pi = AiXORBi$

$Gi = AiBi$

Pi and Gi depend only on the input bits and thus valid after one gate delay.

The sum and carry outputs can be written as

$Ci + 1 = Gi + PiCi$

$Si = Ci\ (XOR)\ Ai\ (XOR)\ Bi$

So, Ci+1 is a function of inputs and Ci

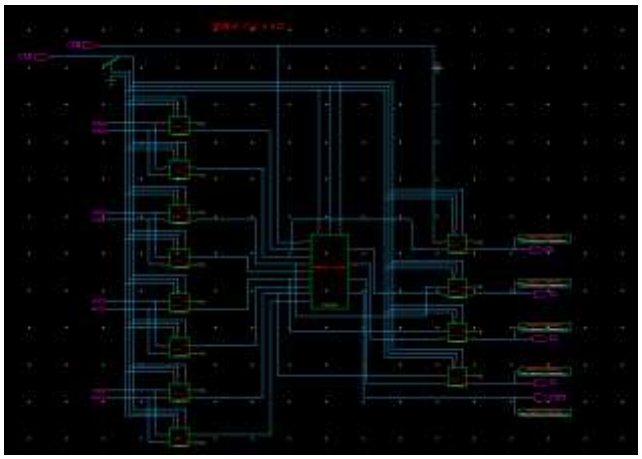
These equations tell that carry signal will be generated into 2 cases:

(a) If both bits Ai and Bi and are 1.

(b) If either Ai or Bi is 1 and carry-in (Ci) is 1.

IV. RESULTS AND DISCUSSION

1) Existing methods



Schematic Diagram of 2N2N2P adiabatic CLA Adder design

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Power Results

V1 from time 0 to 1e-007
Average power consumed -> 9.952966e-006 wa
Max power 3.376364e+001 at time 2e-008
Min power 2.644785e-011 at time 1.20001e-0
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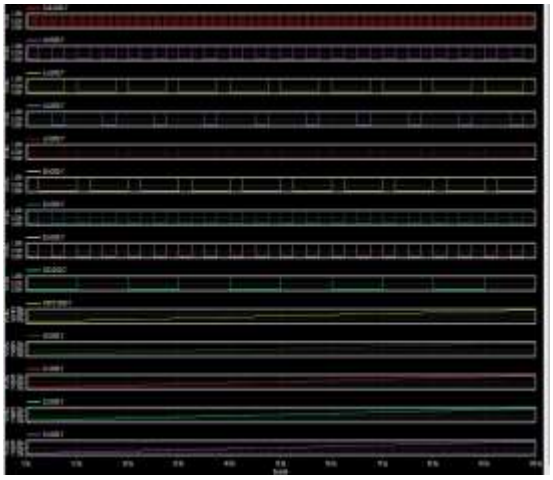
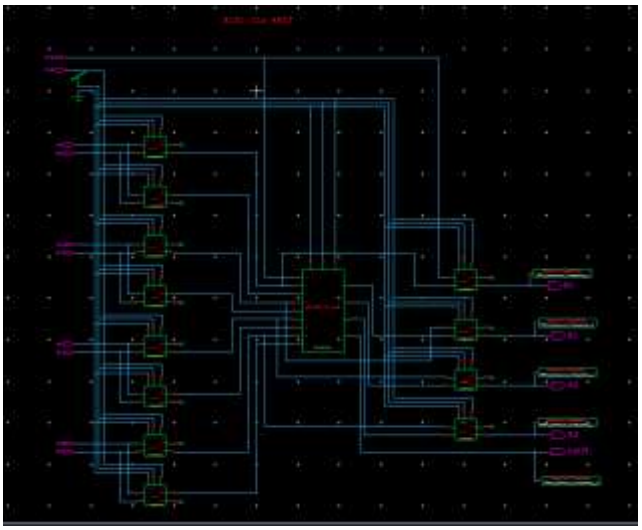
Power and Delay results for 2N2N2P adiabatic CLA Adder design



Output Waveform for 2N2N2P adiabatic CLA Adder design



Schematic Diagram of 2N2N2P adiabatic CLA Adder design

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Power Results

V1 from time 0 to 1e-007
Average power consumed -> 4.659740e-005 watts
Max power 1.198517e+001 at time 2e-008
Min power 1.267897e-008 at time 0
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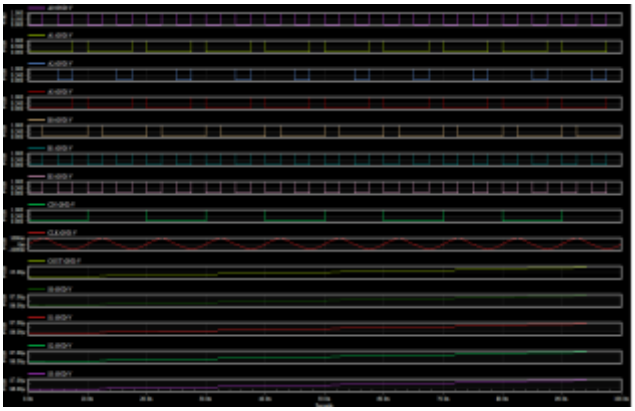
Power and Delay results for 2N2N2P adiabatic CLA Adder design



Output Waveform for 2N2N2P adiabatic CLA Adder design

2) PERFORMANCE EVALUATION

Parameters	2N2N2P	ECRL	2PASCAL
Power	9.95E-05	4.66E-05	4.77E-06
Transistors Count(Area)	378	356	328

Power dissipation of a 2N2N2P and ECRl adiabatic techniques are calculated using Visualization and analysis Tanner EDA tool. Table shows the average dynamic power dissipation comparison 4-Bit carry look ahead adder using static ECRL, 2N2N2P structures.

V. CONCLUSION

In this paper we have implemented two-phase clocked adiabatic CMOS logic (2PASCL) circuits and observed how it works in different phases of input power clock. The simulation results show that power consumption in the 2PASCAL NOT, NAND, NOR, XOR and 16 bit carry-lookahead adder circuits are considerably less than that in a static CMOS adder.

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