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Low Power Quasi Cyclic Approach Based Test Pattern Generation Using BIST Schemes

N. Suganthi

Abstract—Testing of VLSI chips and power consumption is a challenging issue so we proposed the low power quasi cyclic approach based test pattern generation scheme for further power reduction. A Test Pattern Generator (TPG) is used for generating different test patterns in Built-In Self-Test (BIST) schemes. This work generates Multiple Single Input Change (MSIC) vectors in a pattern, applies each vector to a scan chain is a Single Input Change (SIC) vector. A MSIC-TPG and Accumulator based TPG are designed and developed a reconfigurable Johnson counter and a scalable SIC counter to generate a class of minimum transition sequences. The Test Pattern Generator is flexible to both the test-per-clock and the test-per- scan schemes.A theory is also developed to represent and analyze the sequences and to extract a class of MSIC sequences. Analysis results show that the produced Multiple Single Input Change sequences have the favorable features of uniform distribution and low input transition density. It also achieves the target fault coverage without increasing the test length. The architecture modifies scan-path structures, and let the Circuit under Test (CUT) inputs remain unchanged during a shift operation. Compared with the MSIC-TPG, the proposed Accumulator based TPG achieves reduced area and average power consumption during scan based tests and the peak power in the CUT. A low power quasi cyclic approach based test pattern is proposed. The quasi cyclic approach is an efficient technique to reduce the power consumption in the design. For this work, Modelsim 6.2c is used for RTL simulation and Xilinx ISE 13.1i is used for RTL synthesis. The system has been implemented using FPGA SPARTAN3A board.

Keywords **-** Built-In Self-Test (BIST); Test Pattern Generator (TPG); Multiple Single Input Change Vector (MSIC); Quasi Cyclic Approach

I. INTRODUCTION

BIST is a design-for-testability technique that places the testing functions physically with the circuit under test (CUT). The basic BIST architecture requires the addition of three hardware blocks to a digital circuit: a test pattern generator, a response analyzer, and a test controller. Thetest pattern generator generates the test patterns for the CUT. Examples of pattern generators are a ROM with stored patterns, a counter, and a linear feedback shift register (LFSR). A typical response analyzer is a comparator with stored responses or an LFSR used as a signature analyzer. It compacts and analyzes the test responses to determine correctness of the CUT. A test control block is necessary to activate the test and analyze the responses. However, in general, several test-related functions can be executed through a test controller circuit. A digital system is tested and diagnosed during its lifetime on numerous occasions. Such a test and diagnosis should be quick and have very high fault coverage. One way to ensure this is to specify such a testing to as one of the system functions, so now it is called Built Sin Self Test (BIST). With properly designed BIST, the cost of added test hardware will be more than balanced by the benefits in terms of reliability and reduced maintenance cost. For BIST, we would require that the test patterns be generated on the system/chip itself. However, this should be done keeping in mind that the additional hardware is minimized. One extreme is to use exhaustive testing using a counter and storing the results for each fault simulation at a place on the chip (like ROM). An n input circuit would then require 2^n combinations which can be very tiresome on the system with respect to the space and the time. Also, more the number of transitions, the power consumed will be more.The weighted random pattern test is then divided into groups, where each group is activated with a different set of weights. The weights are dynamically adjusted during the course of the test to "go after" the remaining untested faults. An accumulator-based 3-weight test pattern generation scheme is presented; the proposed scheme generates set of patterns with weights 0, 0.5, and 1. Since accumulators are commonly found in current VLSI chips, this scheme can be efficiently utilized to drive down the hardware of built in self test pattern generation, as well. The proposed quasi cyclic approach is an efficient technique to reduce the area and power consumption further in the design. Comparisons with previously presented schemes indicate that the proposed schemerequires less hardware.

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II. DESIGN OBJECTIVES

To design a fault free circuit containing the following features:

1. Circuit under test (CUT) is to be tested using quasi-cyclic approach based test pattern generator
2. TPG is used to generate the test stimulus for the CUT
3. Quasi-cyclic encoder is used to generate the quasi-cyclic test patterns
4. If the circuit has fault, it gives different patterns on the testing circuit
5. If the circuit is fault free, it gives same patterns on the testing circuit

III. EXISTING SYSTEM

A. Accumulator – Based Pattern Generation

A new weighted random pattern design for testability is described where the shift register latch is distributed throughout the chip is modified so that they can generate

biased pseudo-random patterns upon demand. A two-bit code is transmitted to each weighted random pattern shift register latch to determine its specific weight. The weighted random pattern test is then divided into groups, where each group is activated with a different set of weights. The weights are dynamically adjusted during the course of the test to "go after" the remaining untested faults.

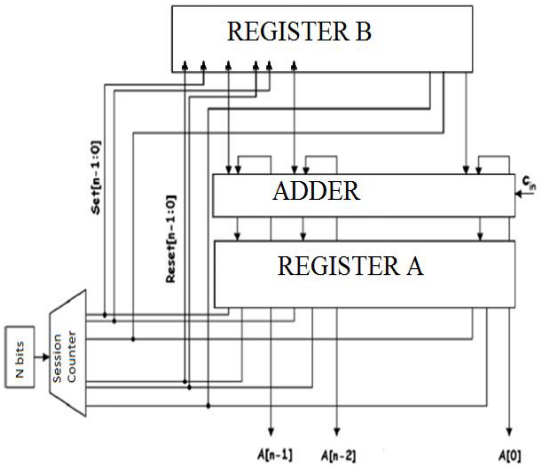

Fig.3.1 Accumulator Architecture

An accumulator-based 3-weight test pattern generationscheme is presented. The proposed scheme generates setof patterns with weights 0, 0.5, and 1. Since accumulatorsare commonly found in current VLSI chips, this schemecan be efficiently utilized to drive down the hardware ofbuilt in self test pattern generation, as well.Comparisons with previously presentedschemes indicate that the proposed scheme comparesfavorably with respect to the required hardware.Accumulator architecture for proposed system is given inthe Fig 3.1.

Fault Detection

Inputs from the Johnson counter are given to the TPG as shown in Fig.4.2. The output of the TPG is given to the S344 (CUT). If the circuit has fault, it gives different patterns on the testing circuit and if the circuit is fault free, it gives same patterns on the testing circuit. Both fault and fault free circuits are analyzed using the analysis circuit.

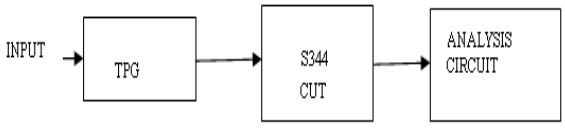

Fig.3.1.1 Block Diagram of Existing System

B. Weight Pattern Generation

The implementation of the weighted-pattern generation scheme is based on the full adder truth table, presented in Table 1. From Table 1, we can see that in lines #2, #3, #6, and #7 of the truth table, Cout = Cin. So, to transfer the carry input to the carry output, it is enough to set A[i] =NOT (B[i]). The proposed scheme is based on this observation. The implementation of the proposed weighted pattern generation scheme is based on the accumulator cell presented. Figure 4.3 consists of a Full Adder (FA) cell and a D-type flip-flop with asynchronous set and reset inputs whose output is also driven to one of the full adder inputs.

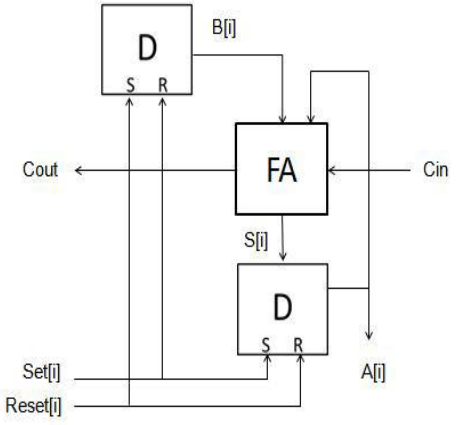

Fig.3.2 Accumulator Cell

#	Cin	A[i]	B[i]	S[i]	C_{out}	Comment
1	0	0	0	0	0	
2	0	0	1	1	0	$C_{out}=C_{in}$
3	0	1	0	1	0	$C_{out}=C_{in}$
4	0	1	1	0	1	
5	1	0	0	1	0	
6	1	0	1	0	1	$C_{out}=C_{in}$
7	1	1	0	0	1	$C_{out}=C_{in}$
8	1	1	1	1	1	

Table 1 Truth Table of Full adder

In Figure 3.2, we assume, without loss of generality, that the set and reset are active high signals. In the same Figure 4.3, the respective cell of the driving register B[i] is also shown. For this accumulator cell, one out of two configurations can be utilized. Here we present these configurations that drive the CUT inputs. 1.For A[i] =1 , We give set[i]=1 and reset[i]=0 and hence A[i]=1 and B[i]=0. Then the output is equal to 1,andCin will be equal to Co. Cin is transferred to the Cout. 2.For A[i] =0 , We give set[i]=0 and reset[i]=1 and hence A[i]=0 and B[i]=1. Then the output is equal to 0, and here Cin is equal to Cout. Cin is transferred to the Cout.

IV. PROPOSED SYSTEM

A. Quasi Cyclic Approach-Based Pattern Generation

Here the quasi cyclic concept is adopted to reduce the power consumption further. In general the power consumption is constituted by the switching activities in the circuit and due to the static operations. In the existing work, the power consumption is reduced using the single input change test

vectors. This means that, there will be a single change/transition from one test vector to another test vector. Due to this single input change mechanism, most of the switching activities are reduced; hence the power consumption is reduced.

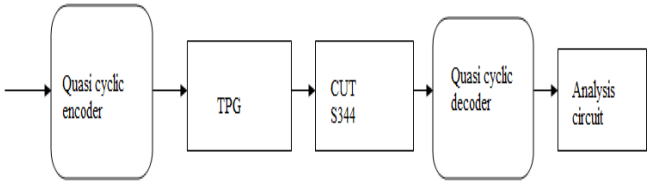

Fig.4.1 Block Diagram of Proposed System

Inputs from the Johnson counter are given to the quasi cyclic encoder as shown in Fig.3.1. The output of the quasi cyclic encoder is given to TPG. The TPG used to generate different test patterns and the test patterns are given to S344 (CUT). If the circuit has fault, it gives different patterns on the testing circuit and if the circuit is fault free, it gives same patterns on the testing circuit. Then it is given to the quasi cyclic decoder. Both fault and fault free circuits are analyzed using the analysis circuit.

B. Quasi Cyclic Encoder

In quasi cyclic approach the logic '1' is encoded as quasi logic '1'. This means quarter of the logic-1 is transmitted. Here we are reducing the time period of the logic-1 value.

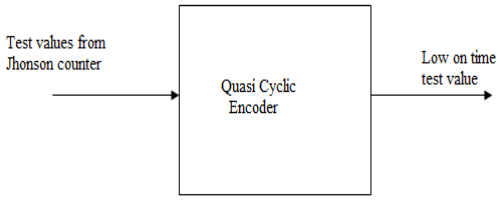

Fig.4.1.1 Quasi Cyclic Encoder

C. Quasi Cyclic Decoder

Here in quasic cyclic mechanism, we are reducing the static time of input duration.ie. Logic-1 is time duration is reduced to quarter amount of the clock. In this way we are reducing the power consumption further. The below figure illustrates the quasi cyclic mechanism.

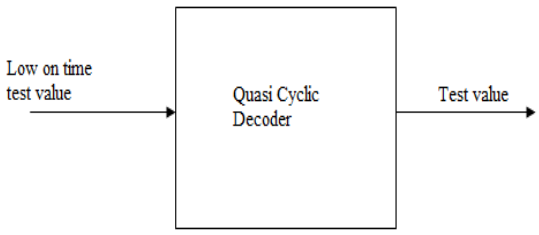

Fig.4.1.2 Quasi Cyclic Decoder

V. SIMULATION RESULTS

Modelsim is a simulation tool for hardware design which provides behavioral simulation of a number of languages, i.e., Verilog, VHDL, and System C. Verilog HDL is an industry standard language used to create analog, digital, and mixed-signal circuits. Verilog code is generated for this accumulator circuit using 6.4c.Then RTL schematic is produced using XILINK 13.2. These test patterns are implemented in FPGA SPARTAN 3.

COMPARISION TABLE

Table 2 Comparision of Area and Power

COMPARISION TABLE	AREA(m^2)	POWER(W)
ACCUMULATOR BASED TPG TECHNIQUE	139	0.184
QUASI CYCLIC APPROACH BASED TPG TECHNIQUE	86	0.128

In this work area and power reduction is done by Xilinx ISE 13.2 version software. The Accumulator based TPG technique produce area of 139m2 and for this, the corresponding power is 0.184w. Now the Quasi cyclic approach based TPG technique produces reduced area of 86m2 and the corresponding power is reduced to 0.128w. The comparision results are tabulated in Table 2 and validated that The Quasi cyclic approach based TPG has reduced area and power compared to Accumulator based TPG.The output waveform of pattern generator, quasi cyclic encoder and quasi cyclic decoder as shown below.

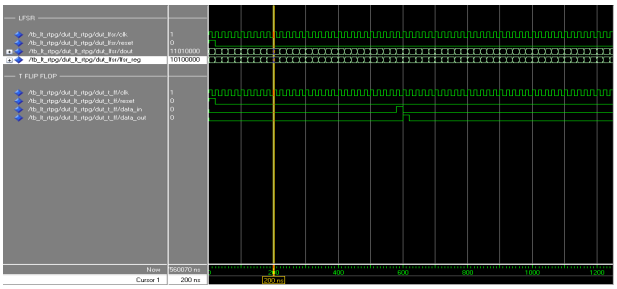

Fig.5.1 Waveform of Test Pattern Generator

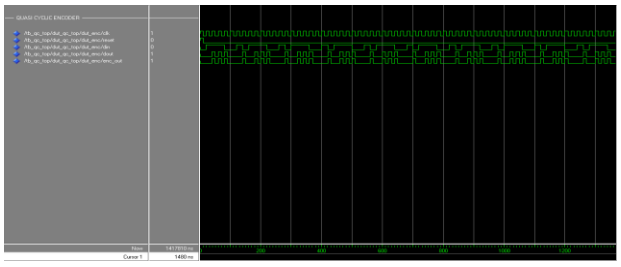

Fig.5.2 Waveform of Quasi cyclic Encoder

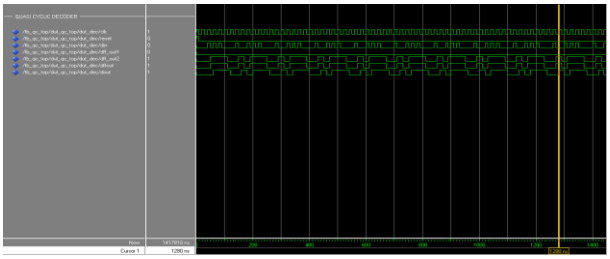

Fig.5.3 Waveform of Quasi Cyclic Decoder

VI. CONCLUSION AND FUTURE WORK

Compared to the Accumulator based TPG technique the Quasi cyclic approach based pattern generation technique has less fault coverage and lower hardware overhead. The hardware overhead of the proposed scheme is lower (75%). The testing time is also reduced to 20%–65%while at the same time no redesign of the system is imposed. Finally, the quasi cyclic approach based technique produces less Area and Power compared to the Accumulator based TPG technique. In the future, more refined methods for obtaining the controlled transition density mixing in the vector set, generated from LFSR by using linear programming approach is to be examined simultaneously to reduce the test time and test power more efficiently.

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