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Low power transition delay fault pattrn generation using LOC and BS-LFSR

M.Vignesh, J.Jayaseelan

***Abstract*—** In IC manufacturing there are many faults are disturbing the quality of the chips, one of the major fault is transition faults. In this paper mainly focusing on to reduce the transition faults with low power. In existing method for finding the transition faults is test cube merging; by using this technique low power test patterns are achieved. In this paper proposed two techniques named as BS-LFSR and launch-off-capture (LOC) test are analyzed based on area, power and delay for transition faults. In BS-LFSR, which generate PseudoRandom pattern with reduced switching transition that occur in the output stream of LFSR, so because of transition reduction low power test generation achieved .In launch-off-capture test, the controllability of the transition fault testing is increased with low power manner. Experimental results for ISCAS'89 S27 benchmark circuits proves which technique is better than the existing technique by reducing power and also compare the area and delay.

***Keywords*—** ATPG-Automatic Test Pattern Generation BS-Bit Swapping, BS-LFSR-Bitswapping Linear Feedback Shift Register, CUT-Circuit Under Test, LFSR- Linear Feedback Shift Register,LOC-Launch-Off-Capture,VLSI-Very Large Scale Integration,SOC-System On Chip.

I. INTRODUCTION

In VLSI technology one of the major problems is the power consumption, now days Engineers are trying to reduce the power consumption in many ways [2]. VLSI testing is the major one in the IC process it is used to find the faults in IC. In VLSI one of the major problems is high power consumption; this is mainly due to the high switching transition because of the transition faults .In this paper targeting the transition faults with low power. The transition fault model targets each gate output in the design for a slow-to-rise and slow-to-fall delay fault. Transition fault testing is mainly practiced in industry due to reduce or manage the fault count .In testing, test patterns are generated through the ATPG tool and it is applied to the CUT (circuit under test) and finds the faults. In that test pattern generation is consuming the high power, one of the main reasons is high switching activity, so if the switching activity is reduced then power consumption will reduce [8].

For reducing the power consumption in testing by reducing the switching activity, there are many techniques [1][7] are used before. The one of the procedure is based on merging of test cubes from the conventional LFSR. The use of test cube merging supports test compaction and it can be used for accommodating the constraints of test data compression. The use of functional broadside test provides a target for the switching activity of low power test, which does not exceed the switching activity that is possible during functional operation. Merging test cubes achieve test compaction. The number of transition in the scan chain can be minimized. But it will increase the complication. In this paper we are going to compare the performance of 2 techniques BS-LFSR (bit swapping linear feedback shift register) and LOC (launch-off-capture) for the transition faults. And finally this paper will conclude which technique is better, based on the performance comparison of area, power and delay.

BS-LFSR (Bit Swapping-Linear Feedback Shift Register) is the modified form of conventional LFSR .The bit swapping technique is used in the output of the normal LFSR; it consists of normal LFSR and 2*1 Multiplexer. Next technique is LOC (Launch-off-capture) for transition fault testing; it has 3 cycles initialization cycle, launch cycle, capture cycle. By using these two techniques we are going to compare which one will achieve low power better than the other techniques by also compare the area and delay.

M.Vignesh is with Department of Electronics and Communication Engineering, Parisutham Institute of Technology and Science, Thanjavur, Tamil Nadu, India, (vignesh209@gmail.com)

J.Jayaseelan is Assitant professor, Department of Electronics and Communication Engineering, Parisutham Institute of Technology and Science, Thanjavur, Tamil Nadu, India

II. LITERATURE SURVEY

The transition faults are detected by using many techniques and here we are going to see about the survey. Static compaction technique [9] [10] is used, it will merge the two test cubes, advantages are low power is achieved and test cube count will be reduced but some disadvantages are there average number of transition is increased and delay will increased.

Judicious utilization of logic [6] is used that means that insertion of logic gates between the scan cells, the main advantages are transition are reduced and low power consumption is achieved, disadvantages are test time is increased and then area will be increase.

LS-TDF [3] and FLIS calculation are used here high switching patterns are filtered and replace the low switching patterns , advantages are switching transition is reduced and low power will be achieved but the disadvantages are test time increased and test patterns count are increased .

Layout aware compaction technique [5] used it will generate the evenly distributed switching activity in the patterns. Advantages are fault coverage increased and delay failures reduced and disadvantages are test pattern count and power is increased.

Test data compression technique [4] is used to combine the MT FILL and VPRL code, advantages are data volume

decreased and power reduced disadvantages are added complication and effect of errors in transmission.

In proposed paper used two techniques BS-LFSR and LOC by using this proposed technique we will achieve the low power comparing to the previous technique and then finally we will compare the area and delay based on the result we will conclude which technique is better comparing to the previous technique.

III. Existing System

In existing technique test compaction procedures are used. It is used to compress the data .In this test compaction, mainly we are merge the test cubes. LFSR generates the test cubes for transition faults and finally we merge them for achieve the test compaction. The main goal of the existing and our proposed paper is to achieve the low power. Merged test cubes will find the same set of faults; it will not affect the fault coverage. Test cubes are extracted from the functional broad side tests.

First fully specified functional broad side test set is generated. And it is not a low power test set .Test cubes are extracted from it for the transition faults. Then the test cubes are preserving some signal transition of the broadside test, from which they are extracted.

The switching transition will increase the power consumption, so this existing test cube merging is mainly focused on switching activity. 0s and 1s changes in the test set are called the switching transition. Because of merging the test cubes the switching transition will decrease in the system finally we will get the low power consumption.

In our proposed system, we are using 2 techniques BS-LFSR and LOC; it will reduce the switching activity better than the test merging technique, so we will get low power compared to the existing.

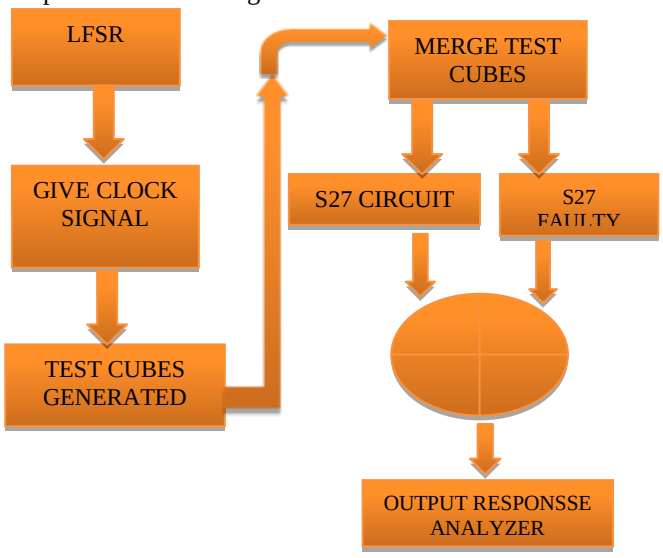

Figure 1: Test Cube Merging

IV. BS-LFSR Test Pattern Generation

A. Conventional LFSR Test Pattern Generation:

In normal test pattern generation, LFSR is formed by XOR and flip flop. It performing XOR on the output of the two or more flip flop and then feeding those outputs back in to the input of one of the flip flop and it generate the PRPG , clock signal is the important one in the LFSR for test pattern generation.

B. Modified LFSR Test Pattern Generation:

In the modified LFSR it consists of conventional LFSR and 2*1 Multiplexer. BS-LFSR will reduce the switching transition comparing to the conventional techniques so we are achieving the low power. Switching transition will normally consume more power in the conventional LFSR but in the proposed BS-LFSR it will be decrease. So this is the one of the main advantage in BS-LFSR, for that we are using the 2*1 multiplexer in the architecture.

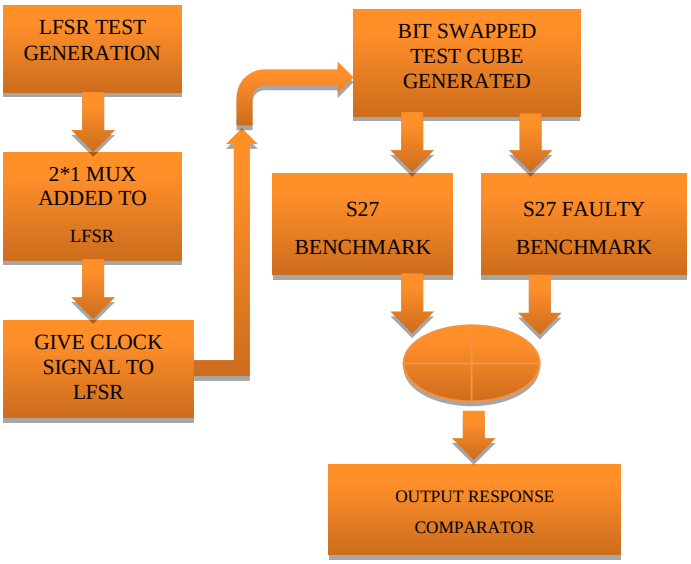

Figure 2: BS-LFSR Architechture

Figure 1 diagram shows the architecture diagram for the Bit Swapping Linear Feedback Shift Register. It reduces the average switching activity in test operation by reducing the number of switching transition.

Bit Swapping LFSR design is based on some procedure that is used to describe the switching transition activity in BS-LFSR. By using this procedure we can easily define how switching transition of bits takes place in pattern generation.

There are many techniques to reduced power consumption there is some direct techniques are there for reducing power but it will increase the timing of test and are not applicable for reducing peak power. Bit-Swapping LFSR will reduce both average and peak power dissipated by CUT.

In modified LFSR we apply the swapping property between the every pair of adjacent cells of the normal LFSR for design the BS-LFSR. In the n-bit maximal length LFSR is modified using the swapping arrangement, we choose one of its output is to be a selection line that will swap the two neighboring bits.

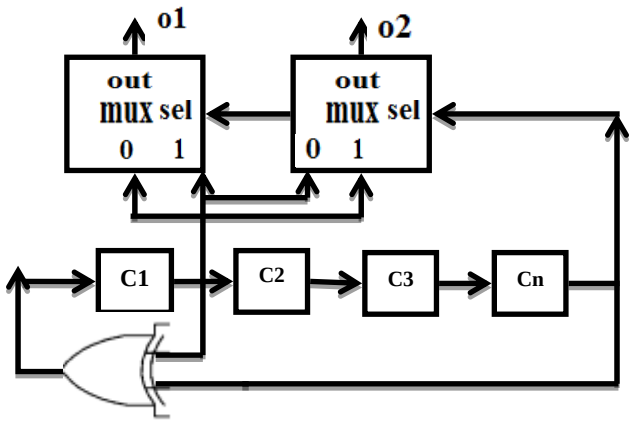

Figure 3: Bit-Swapping Lfsr

C. Properties:

1. *Modified LFSR will generate the exactly same as the normal LFSR but the test pattern generated order will be different.*
2. *BS-LFSR generate same number of 0s and 1s in the output of multiplexers after swapping of two adjacent cells*
3. *BS-LFSR is used to generate test patterns for the primary inputs of a scan-based sequential circuit. Then consider that bit1 will be swapped with bit2 and bit3 will be swapped with bit4…….. bit n-2 with bit n-1 according to the value of bit n which is connected to the selection line of the multiplexer.*
4. *For n-bit maximal length LFSR that starts with any seed and runs for 2n clock cycles until it returns to the starting seed value.*
5. *Then the total number of transitions is*
6. *T total = n*2(n-1)(1)*
7. *So after swapping the swap bit will therefore save power.*
8. *T saved =2 (n-2)/ (2*2(n-1))=25%*
9. *The overall transition in the primary input of the CUT will be reduced 25%.*

V. LOC(LAUNCH-OFF-CAPTURE)

In this paper we proposed two techniques BS-LFSR and LOC. Now we are going to see about launch-off-capture. The LOC method is for finding the transition faults, in this method utilizes the functional response of the circuit to launch the transition at a target gate terminal and propagate the fault effect to an observable point.

The main goal of this paper is to reduce the power consumption. By using the LOC method power consumption is reduced during launch and capture operations in at- speed testing. This method is to reuse the patterns generated by a conventional power unaware transition delay ATPG tool intact and apply them in a low power manner.

The transition fault and path delay fault testing provide a good coverage for delay induced defects. Transition fault model targets each gate output in the design for a slow to rise and slow to fall delay fault. Transition fault testing widely used in industry for mainly to manage and control the fault count.

To test a transition fault, a pattern first is applied to initialize the circuit and another pattern is used to apply a transition at a target terminal. The response is observed at the outputs of the CUT (circuit under test). The scan based test generated by an automatic test pattern generator (ATPG) is mainly used as a cost effective alternative to the at-speed functional pattern approach. LOC is going to perform the transition fault test in scan based method, a pattern pair V1 and V2 is applied to the circuit-under-test. First pattern V1 is termed as the initialization pattern and V2 is termed as the launch pattern.V2 launches the signal transition (0 to 1 or 1 to 0) at the desired node. It also helps to propagate the output transition to the output of CUT (primary outputs or scan flip flops). The response of the circuit under test for the pattern V2 is captured at the functional speed. The total operation can be divided in to the 3 cycles: 1. Initialization cycle, where the CUT is initialized to the particular state (V1 is applied) ,

2. Launch cycle where the transition is launched at the target gate terminal (V2 is applied), and finally 3. Capture cycle, where the transition is propagated and captured at an observable point.

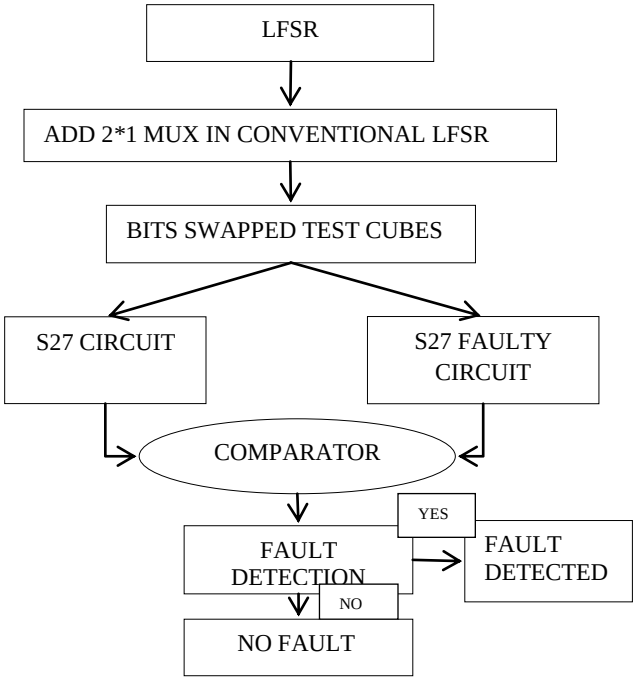

Figure 4: Flow Char For Bs-Lfsr

VI. ISCAS 89' – S27 BENCHMARK CIRCUIT:

In this paper we are using S27 circuit, which belongs to ISCAS 89' benchmark circuit family and it is purely sequential circuit with four inputs. The circuit has been tested by using Built In-Self Test. Initially faults are inserted in to the circuit. For each and every fault pseudorandom patterns

are applied corresponding test vector will be taken. These vectors are divided in to two sub groups for reduction of transitions. The number of transitions are reduced the power consumption is reduced. If the output value of faulty S27, and S27 normal circuit are different then fault has been covered.

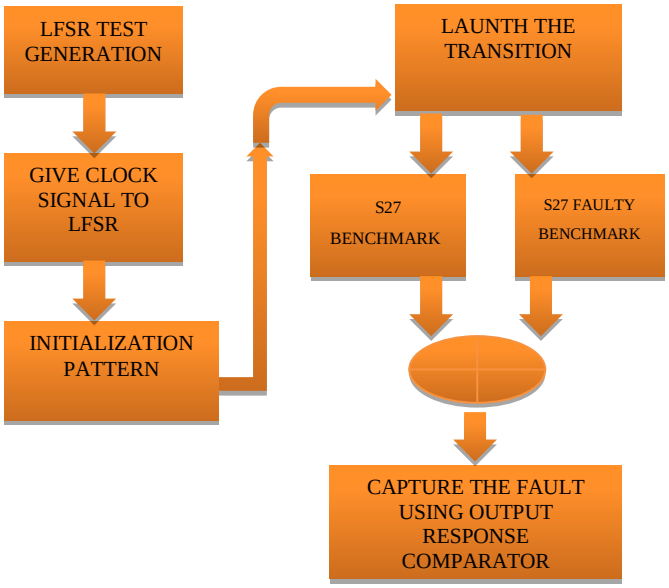

Figure 5: LOC- Launch-Off-Capture Architecture

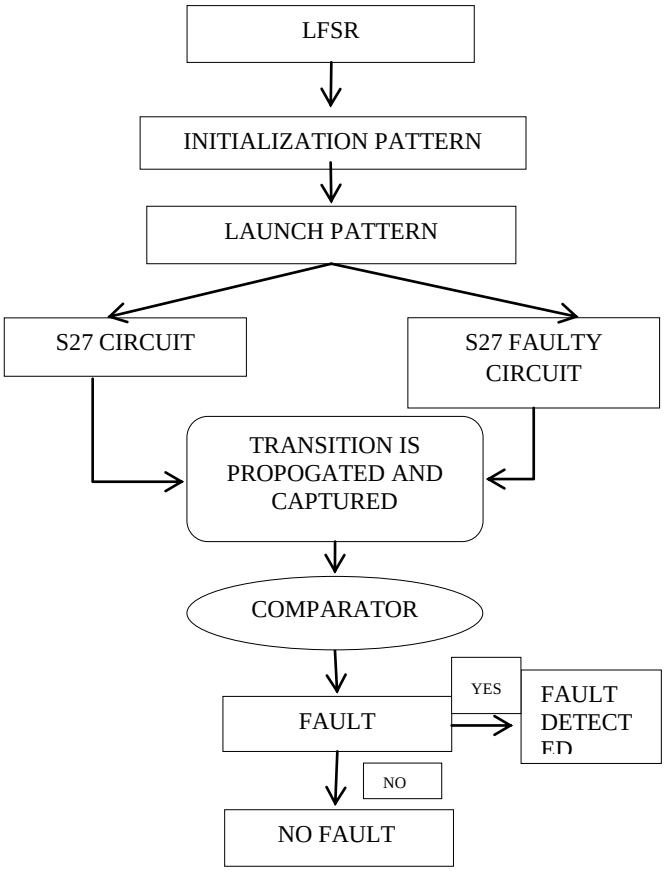

Figure 6: Fiow chart for LOC

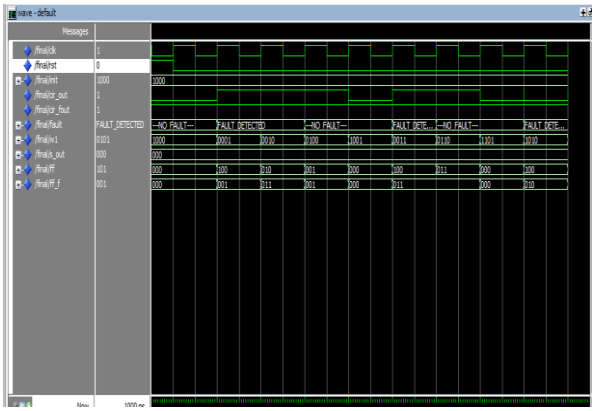

Figure 7: fault detection output using modelsim

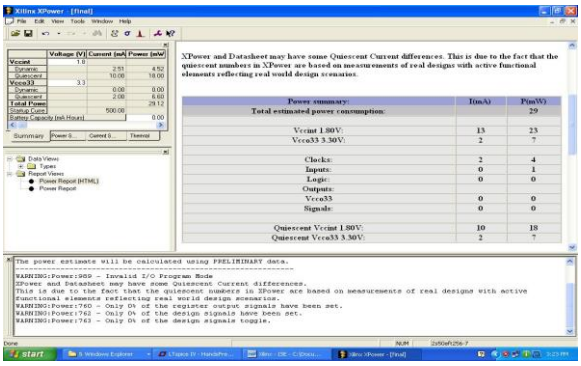

Figure 8: Total Power Mesasurement For Test Merging Using Xilinx

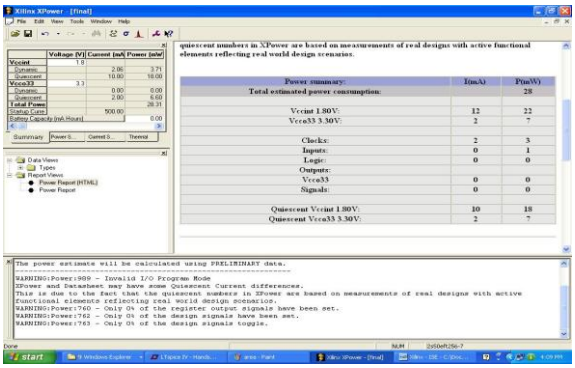

Figure 9: Power Consumption Measurement Using Xilinx for BS-LFSR

VII. EXPERIMENTAL RESULTS:

In this paper we are using VHDL program, and we are going to use two software, MODELSIM, and Xilinx. ModelSim tool is used for measuring the accurate fault detection, and Xilinx tool is used for measuring the area, power and delay .We are using ISCAS 89' S27 benchmark circuit. We are expecting further reduction in power comparing to the test merging technique. And within these two proposed technique which is giving better result in area

and delay comparison then we will finalize which one is better than the existing technique. Then figure 7 shows the fault detection using modelsim, it is accurately detect the faults. And figure 8,9 shows that the power measurement using the Xilinx. Total power consumption for test merging is 29mw and for BS-LFSR 28mw so power reduction is proved and we need to find power for LOC and compare the power then we conclude which one is better than the existing. In our proposed system we will reduce further reduction in power using BS-LFSR and LOC.

VIII. CONCLUTION AND FUTURE WORK

In this paper we are generated the test patterns for transition faults using this proposed two technique BS-LFSR and LOC. In BS-LFSR Bit Swapping technique is applied to the conventional LFSR and we used 2*1 multiplexer then in LOC we are split the operation in 3 cycles initialization cycle, launch cycle, capture cycle. By using these 2 proposed technique we are going to achieve the low power and comparing the area and delay with power then finally prove which one is better than the test merging technique for that we used ISCAS 89' – S27 Benchmark circuit.

BS-LFSR achieve low power comparing to the existing technique and future work is we need to find the measurement for power , area , and delay for LOC and we will compare which one is better comparing to the existing technique.

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REFERENCES

[1] Anshuman Chandra and Krishnendu Chakrabarty "A Unified Approach to Reduce SOC Test Data Volume, Scan Power and Testing Time*" IEEE Trans. Comput.-Aided Design*, Vol. 22, no. 3, March 2003

[2] Chetan Sharma "Power Reduction in VLSI chips by Optimizing Switching Activity at Test Process, Architecture & Gate Level*." International Journal of Engineering Science and Technology (IJEST),* Vol. 3 No. 4 April 2011, PP-3256-3259.

[3] Jiann-Chyi Rau, Po-Han Wu and Wei-Lin Li "Test Slice Difference Technique for Low-Transition Test Data Compression*" Journal of Applied Science and Engineering,* Vol. 15, No. 2, PP-157-166 (2012)

[4] Jeremy Lee and Mohammad Tehranipoor "LS-TDF: Low-Switching Transition Delay Fault Pattern Generation *" 26TH IEEE Test Symposium,* 2008,PP-227-232.

[5] J. Lee, S. Narayan, M. Kapralos, and M. Tehranipoor, "Layout-aware,IR-drop tolerant transition fault pattern generation," in *IEEE Proc. Design, Autom. Test Eur. Conf.*, 2008, pp. 1172–1177.

[6] Kuen-Jong Lee, Shaing-Jer Hsu and Chia-Ming Ho "Test Power Reduction with Multiple Capture Orders*" IEEE Proceedings of the 13thAsian Test Symposium* , 2004., PP-1-4.

[7] Lee Whetsel "Adapting Scan Architectures for Low Power Operation" *IEEE ITC International Test Conference*, 2000, PP- 863-872.

[8] L. Whetsel, "Adapting scan architectures for low power operation," in *IEEE Proc. Int. Test Conf.*, 2000, pp. 863–872.

[9] Ranganathan Sankaralingam, Rama Rao Oruganti, and Nur A. Touba "Static Compaction Techniques to Control Scan Vector Power Dissipation" . *18th IEEE VLSI Test Symp., May 2000 ,pp 35-40,.*

[10] R. Sankaralingam, R.R.Oruganti, and N.A.Touba, "Static compaction Techniques to control scan vector power dissipation," in *Proc. 18th IEEE VLSI Test Symp* , May 2000, pp. 35–40.

M.VIGNESH received degree B.E (ECE) from Periyar Maniammai University, Thanjavur, Tamilnadu, in 2012. He is currently persuading M.E-VLSI DESIGN in Parisutham Institute of Technology and Science, Thanjavur, Tamilnadu, India, (affiliated to Anna University Chennai).