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Partitioning Three Dimensional IC in Circuit Level

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Abstract— More number of Silicon die has been vertically stacked and allowed for three dimensional Integration. Using Silicon Vias the stacked die are strongly integrated. Short Vertical Connections used in die are replaced with long global wires. Previous work has been represented only general test architecture for pre bond testability. This work proposes new methods for partitioning only at circuit level. The individual Circuits having gates and circuits could be split across die layers. We are using port split register unit and adder unit. For every circuit three dimensional view, Planar and layouts are produced. Our paper verifies power measurements, Performance, Monitor the Coverage of testing.

Index Terms- Design for Testability, Die Stacking,3D ICs, Memory Test, Built In Self Test.

I. INTRODUCTION

As the IC industry continues the push to smaller and smaller device geometries, the cost of each new process generation is steadily on the rise while the returns continue to diminish. In an effort to keep up with Moore's Law in spite of these difficulties, manufacturers are increasingly turning to new fabrication technologies. 3D integration is one such technology which allows for the integration of multiple silicon die into a single chip stack. Vertical integration is completely orthogonal to device scaling, making it an excellent complementary technology to help keep Moore's Law on track for at least another decade.Previous works on 3D design have studied a number of different partitioning schemes [3, 4, 9, 14, 10]. These designs range from simply stacking SRAM die on top of a processor die (to form a massive last-level cache) to splitting a single microarchitectural block or even circuit (such as an adder) across multiple die. Some of the latter advanced designs promise increased performance while simultaneously reducing both power consumption and area. However, one major problem remains largely unaddressed: how do we test these individual die before bonding them together to form the complete chip?Note that, without this pre-bond test, a defect in a single die could ruin the entire stack, which reduces manufacturing yield exponentially as the number of die increases. This work proposes and evaluates test strategies for two of the most ambitious 3D designs, a bit-split Kogge-Stone adder and a port-split register file, extending the previous work by Lewis and Lee on a general pre-bond test strategy [8].The rest of this paper is organized as follows. Section 2 introduces 3D technology, explores the contributions of previous work, and the problem addressed in this work; Section 3 will present the 3D designs.we have considered and our extensions to these designs to enable pre-bond testability; Section 4 presents our experimental setup and results; Section 5 discusses related work. Section 6 concludes the paper with a summary and discussion of results.

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II. 3D TESTING & 3D INTEGRATION

3D integration (die stacking) is an emerging technology in which multiple silicon die are stacked and tightly integrated with short, dense die-to-die vias. Designing in the third dimension has many advan-tages. First, it allows for die manufactured in incompatible processes to be tightly integrated—for example, logic and DRAM [3]. Second, it can increase routability [13]. Third, the high density of die-to-die vias can provide a plethora of memory bandwidth, which has been constrained by the pin count on the package. Last, and possibly most important, it can substantially reduce wire length, which in planar die both degrade performance and increase power consumption [14].

3D Technology :-

The general concept of 3D integration. Two die, previously manufactured in any VLSI process, are bonded together with short, high-density die-to-die (d2d) vias. These d2d vias come in two flavors, faceside and backside. Faceside vias, manufactured o n top of the metal interconnect layers, can be produced on a pitch of a few hundred nanometers [15]. Backside vias, also called *through silicon vias* (TSVs), are manufactured through the bulk silicon on a pitch of microns. To keep these TSVs small, the bulk silicon must be thinned, usually with a CMP process, to a few tens of microns. D2d vias on different die are then fused together to bond the die to-gether [12]. A face-to-face bond, is best, providing the shortest, highest density interface. However, stack heights greater than two layers require the use of face-to-back or back-to-back bonds. Once the stack is complete, normal C4 solder bumps can be placed either on TSVs or on top of the metal layers as in a traditional planar design.

3D Partitioning :-

Generally speaking, there are three distinct granularities of 3D par-titioning schemes. The coarsest granularity is the *technology par-titioning*. Disparate technologies, like high-speed CMOS and high-density DRAM, are manufactured in separate, optimized processes and then tightly integrated with 3D technology. This integration al-lows for high-speed, high-

bandwidth interconnections between tech-nologies that simply are not possible with planar manufacturing.The next finer level of partitioning is the architectural level. Here, die are manufactured in the same process. The goal is to partition the microarchitectural blocks across the different layers such that the total wire length is minimized. For example, adders could be stacked, allowing the bypass bus to make short vertical connections instead of long horizontal ones. Architectural partitioning generally makes much better use of the available d2d vias than technology partitioning.The finest partitioning granularity is the circuit level. Here, individ-ual blocks or even individual circuits are partitioned across multiple layers. A large range of possibilities exist at this granularity. At one end of the spectrum is sub-block partitioning where a block is split along logical boundaries. For example, a cache bank could be folded in half, significantly reducing the load on the word- or bit-lines [9, 14]. At the other end, individual circuits are partitioned. For exam-ple, the ports in a multi-ported register file can be partitioned across layers, greatly reducing the area and thus wirelengths of the register file [14]. Such designs make best use of the available d2d vias and thus promise the best improvements in power and performance.

3D Test :-

3D integration suffers from the same problem as multi-chip mod-ules (MCMs), IC boards, and other integration schemes: one bad component can kill the system. As more components are integrated, the yield of the final product falls off exponentially. The solution is to test components before integration, finding so called "known good die" (KGD) parts. We propose this same approach to pre-bond test for 3D integration.At the technology granularity, there is little challenge. Each layer is a complete, functional design that can be tested in a normal planar method (as is done for MCMs). The only challenge lies in the coexis-tance of probe pads for test and d2d vias for 3D integration. But since these designs consume relatively few vias, there is room to spare, so this is really just an engineering problem to be tackled on a per-design basis.At the architectural granularity, things get trickier. Buses that con-nect neighboring blocks in a planar design will likely be non-functional in a pre-bond test situation. Worse, global signals—clock, power, reset, etc.—may not be functional pre-bond. These challenges were partly addressed in previous work by Lewis and Lee [8]. They showed that application of the scan island methodology, first implemented in the Alpha 21364 processor, could sufficiently test blocks pre-bond.Additionally, design options for ensuring power, clock, and reset distribution
pre-bond were presented. However, this work was limited inscope to the architectural granularity and did not consider finer partitions.At the circuit granularity, pre-bond test becomes quite a challenge.Individual transistors from a single circuit may be partitioned across the stack. This leads to a bit of a paradox in that the circuits are functionally broken pre-bond, yet we want to test them for correct functionality. Additionally, the large number of d2d vias in some designs makes traditional scan-based test impractical. To address these issues, we consider two designs: a bit-split Kogge-Stone adder and a port-split register file. The adder represents a sub-block partition where the number of vias is small enough to allow scan-based test. The register files represents the opposite end of the spectrum, and a new test methodology is required. Taken together, these examples demonstrate that the range of circuit-partitioned designs can be practically tested pre-bond.

III. 3D DESIGN AND TEST

Previous work in 3D design has examined different partitioning schemes for key functional units in high-performance microprocessors.These units include caches, instruction schedulers, arithmetic units, and register files [14]. Some of these—the cache designs in particular—involve what is best described as sub-block partitioning.These designs are easily testable using the scan island test strategy in [8]. Others, most notably the port-split register file design, are partitioned at a very fine granularity and seem completely untestable by known techniques.To cover this range of partitioning options, two designs are selected as representative cases. These are the bit-partitioned Kogge-Stone adder and the port-partitioned register file. The Kogge-Stone adder represents the easiest of the circuit-partitioned cases, using only a few internal vias and mostly resembling an architecture-partitioned design (i.e. most functionality is still intact pre-bond). The port-split register file, on the other hand, makes extensive use of internal vias and heavily divides functionality across layers, representing a unique and difficult pre-bond test challenge.

Koggestone Adder

The planar and 3D designs of an eight-bit adder. A Kogge-Stone adder makes heavy use of prefix units to minimize the fanout of each unit and increase addition speed.Prefix values are shifted left after each stage by an exponentially increasing distance to produce the carry values. As the bit count increase to 32, 64, and 128 bits, the wiring costs explode. To alleviate this problem, the 3D design proposes a modulus partitioning of the original operand bits. a modulus two (i.e. odd and even) partitioning; the same partition when stacked.

IV. EXPERIMENTS AND ANALYSIS

Power and Performance

To evaluate our test strategy on these two circuits, planar and 3D versions were implemented in 3DMagic [5], an extension to the open-source Magic VLSI tool [1], that enables the creation of 3D layouts. Both implementations were partitioned across two die layers. Our Kogge-Stone implementation is a full 64 bits To compute a 64-bit sum, the Kogge-Stone adder requires eight lev-els of logic. The first level, located at the top of the layout, computes the generate and propagate signals. The next six levels incremen-

Test Cost and Coverage

To evaluate the test cost and coverage for the Kogge-Stone adder,we used the Mentor Graphics tool set. First, gate-level structural Verilog models of both the 2D and 3D implementations were produced and verified in ModelSim. For the 3D case, we produced three model files: one file

describing the bottom layer, one file describing the top layer, and one file describing the via connections. This division of the model ensured an accurate description of the model was available for both pre- and post-bond test simulation.The actual test simulation was produced using FlexTest. This tool provides a list of faults, a set of test vectors, and the fault coverage achieved. In order to achieve a fair comparison between the planar and 3D cases, we ran three fault simulations for the 3D implementations. The first two targeted all faults within the two independent layer models, simulating pre-bond test. The last simulation targeted faults on the via nets between the two layers, simulating a post-bond test verifying that the two die were successfully bonded. Summing the cost of these three tests estimates the total cost of testing the 3D design fairly.

V.RELATEDWORK

Research in 3D-IC test area is still in the early stage. Make [11]first identified several generic research directions in testing 3D circuits.In [8], Lewis and Lee proposed a scan-island based technique to enable pre-bond test for 3D microprocessors partitioned at the architectural level. Wu *et al.* [16] studied the scan chain ordering in3D ICs for minimizing the total wire length. Jiang *et al.* [6] studied 3D-aware test access mechanisms by taking pre-bond test times into account to optimize the overall test time. More recently, Lee and Chakrabarty [7] overviewed the research challenges to be addressed in 3D-ICs to make them a market success.

VI. CONCLUSION

This work investigated test strategies for circuit-partitioned 3D designs in which a functional unit can be partitioned into incomplete circuits across different die layers. Our techniques present standard scan registers that can be integrated into the layer scan chains, allowing the ATE to (in the standard scan case) directly test the circuit or (in the PRPG/MISR case) initialize the registers for BIST. To demonstrate our methodology, we performed two case studies using a prefixed parallel adder and a register file. In the case of the bit-split 3D Kogge-Stone adder, pre-bond test involved a simple extension to scan-based test. The port-split 3D register file was much more difficult, requiring a new test strategy to enable pre-bond test. Our full layout implementations confirmed the power and performance improvement estimates reported by previous work, and our fault simulations based on detailed Verilog models demonstrated high fault coverage at reduced cost compared to equivalent planar designs. We have shown that even the most difficult 3D partitioning schemes can be tested pre-bond, ensuring the viability of many-layer die stacks.

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