VLSI Implementation of 2 bit Pwm Transceiver Using Sequential Self Reference Edge Detection Techniques

P.Sharmila , A.Bala ganesaram

Abstract— In this paper, the requirement of decreased power supply voltage for CMOS device scaling motivates us to develop time domain circuits. A CMOS pulse width modulation (PWM) transceiver circuit that exploits the self-referenced edge detection technique is presented. By comparing the rising edge that is self-delayed by about 0.5 T and the modulated falling edge in one carrier clock cycle. It has the capability of timing error measurement while changing the length of self delay element are realized. For reliability improvement, Remodel the design of T-Rx Architecture such that 3 bit PWM transceiver then ECC circuit design for 2 bit error recovery. To develop time- domain circuits, and widely used for many applications, such as wireline transceivers, CMOS imagers and biosensor array.

Index Terms - CMOS, jitter, pulse width modulation (PWM), self-referenced, transceiver.

I. INTRODUCTION

Data transmission, digital transmission, or digital communications is the physical transfer of data (a digital bit stream or a digitized analog signal) over a point to point or point to multipoint communication channel.

Examples of such channels are copper wires, optical fibers, wireless communication channels, storage media and computer buses.

Pulse modulation schemes aim at transferring a narrowband analog signal over an analog baseband channel as a two level signal by modulating a pulse wave. Some pulse modulation schemes also allow the narrowband analog signal to be transferred as a digital signal (i.e. as a quantized discrete time signal) with a fixed bit rate, which can be transferred over an underlying digital transmission system, for example some line code.

A. Pulse-width modulation:

Pulse-width modulation (PWM), or pulse-duration modulation (PDM), is a modulation technique used in communications systems to encode the amplitude of a signal into the width of the pulse (duration) of another signal.

The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on and power is being

P.Sharmila, PG Scholar, , Department of Electronics and Communication Engineering, Mohamed Sathak Engineering College, Kilakarai.(Email: sharmigee@gmail.com)

A.Bala ganesaram, Assistant Professor, Department of Electronics and Communication Engineering, Mohamed Sathak Engineering College, Kilakarai. (Email: balaganesaram86@gmail.com)

transferred to the load, there is almost no voltage drop across the switch.

Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle.

II. EXISTING SYSTEM

In the existing system PWM transceiver design requires large-area and power-hungry phase-locked loops (PLLs) for multiphase sampling clock generation.
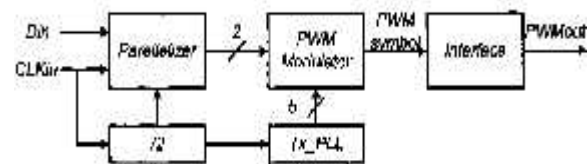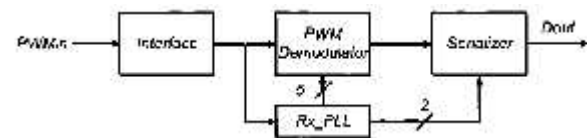

Fig 2.1. Transmitter side

Fig 2.2. Receiver side

The transmitter consists of a parallelizer, a divide-by-two circuit, a PWM modulator, an interface circuit, and a Tx-PLL. The receiver includes a serializer, a PWM demodulator, an interface circuit, and an Rx-PLL.

First, every two bits of the input serial data are parallelized through the parallelizer to form a symbol. That symbol correspond to the pulses with different widths. The PWM-encoded signal is divide- by-two circuit is needed to deal with the bit parallelization. The VCO in the PLL is designed based on a five-stage differential- type ring oscillator and can provide five sets of clock phases for the PWM modulator.

The PWM modulator is periodically triggered by VCO's first set of output signals (in-phase clock) to ensure a synchronous rising edge within a period and reset by another four sets of output signals (out-of-phase clock) depending on the symbols. In this way, a PWM-encoded signal with different pulse widths and synchronous rising edges can be driven out by the interface circuit.

As for the receiver, the process is just the reversal of the transmitter's. The incoming PWM-encoded signal is first converted to signals with full CMOS voltage swing by the

----

receiver's circuits. After that, it is split into two ways. One way is to the PWM demodulator and the other is to the Rx-PLL. The system clock is recovered by the Rx-PLL from the PWM-encoded signals.
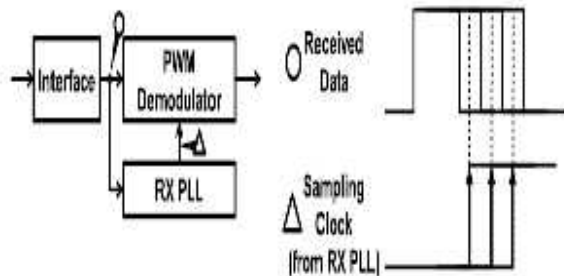
III. PROPOSED APPROACH

Fig 3.1. Conventional PWM receiver in 2 bit PWM.

In proposed system, Rx-PLL is replaced by Self Referenced Edge detector in PWM Tx-Rx Architecture for reduce the power hungry.
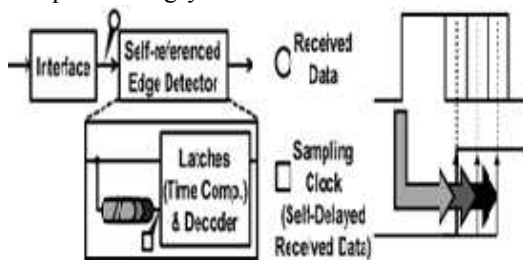

Fig 3.2. Proposed PWM receiver in 2-bit PWM.

The proposed PWM transceiver exploits a timing comparison between the rising edge that is self-delayed by about $0.5T$ and the data-modulated falling edge in one carrier clock cycle, and this mechanism is introduced.

A CMOS pulse width modulation (PWM) transceiver circuit that exploits the self referenced edge detection technique is presented.

3.1.Architecture
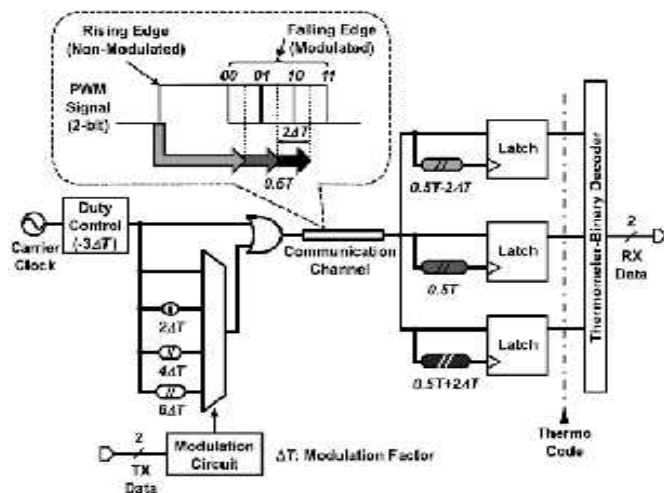
3.1 PWM transceiver architecture

By comparing the rising edge that is self-delayed by about $0.5T$ and the modulated falling edge in one carrier clock cycle.

Self-referenced edge detection circuit has the capability of timing error measurement while changing the length of self delay element, adaptive data-rate optimization and delay-line calibration are realized. For reliability improvement, error check and correction associated with intercycle edge detection is introduced and its effectiveness is verified by 1-bit PWM measurement. Hence, high area efficiency, high speed and low power-consumption.

Transmitter side:

The transmitter consists of a duty controller, four delay elements with length of multiples of modulation factor, T, selector controlled by the PWM modulator, and OR logic.

Receiver side:

The receiver consists of three delay elements with various lengths about a half of the clock period, $0.5T$, latches, and a thermometer-binary decoder.

A conventional PWM receiver exploits a PLL for generating time shifted sampling clocks.

Our newly proposed PWM receiver using a self referenced edge detector employs latches as timing comparators and a thermometer binary decoder. The proposed self referenced edge detection utilizes the self delayed rising edge instead of the PLLs sampling clock.

By comparing this self-delayed rising edge and the data modulated falling edge in one carrier clock cycle, edge detection can be realized. A carrier signal given to duty control ,then 4 different delayed carrier signal and original carrier signal given from output of duty control block.

3.2 ERROR CHECK CODE CIRCUIT

Above all the signal are given to 4X1c UX with one selection bit then signal fed into OR gate then latch get the signal and then comparator take in ECC position then output get from TBD.

Schematic diagram of the ECC circuit for 1-bit PWM. The ECC circuit consists of Two latches ,Mux2x1 and an error detector. ECC utilizes the successive received data from the main receivers, D1 and D2, and data from the auxiliary receivers, A+ and A−.

An error code is generated when a discrepancy between the received data from the main and auxiliary receiver occurs, and the original RX bit is inverted.
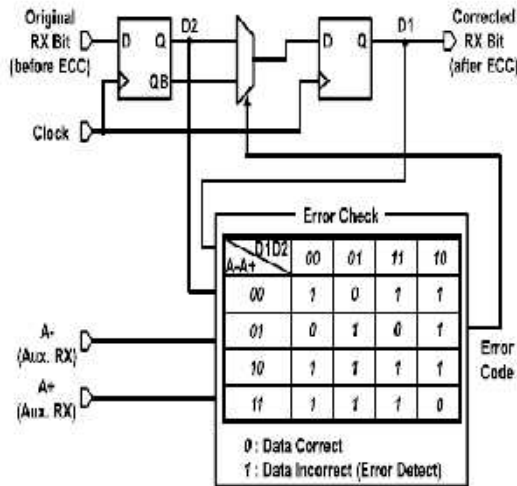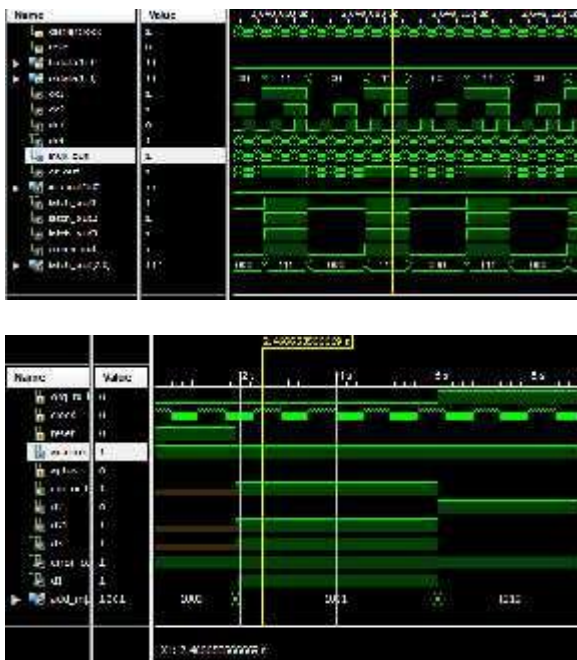

Fig 3.2.1.Schematic diagram of the proposed Error Check circuit

IV. SIMULATION

V. CONCLUSION

A CMOS PWM transceiver circuit using the self-referenced edge detection technique has been demonstrated for the first time. By comparing the self-delayed rising edge and modulated falling edge, edge detection was realized. This edge detection enables area-efficient and high-robustness for PWM communication without exploiting PLLs. The data-rate optimization and ECC with interstage edge detection was introduced. The measured results have demonstrated 2-bit PWM communication, high data rate, high reliability with small area occupation.

REFERENCES

[1] W.H. Chen, G.K. Dehang, J.W. Chen, and S.I. Liu, "A CMOS 400Mb/s serial link for ASmemory systems using a PWM scheme," IEEE J. SolidState Circuits, vol. 36, no. 10, pp. 1498–1505, Oct. 2001.

[2] W.J. Choe, B.J. Lee, J. Kim, D.K. Jeong, and G. Kim, "A single pair serial link for mobile displays with clock edge modulation scheme," IEEE J. SolidState Circuits, vol. 42, no. 9, pp. 2012–2020, Sep. 2007.

[3] C.Y. Yang and Y. Lee, "A PWM and PAM signaling hybrid technology for serial link transceivers," IEEE Trans. Instrum. Meas., vol. 57, no. 5, pp. 1058–1070, May 2008.

[4] M. Takihi, K. Niitsu, and K. Nakazato, "Chargeconserved analogtotime converter for a largescale CMOS bionsensor array," in Proc. IEEE Int. Symp. Circuits and Syst., Jun. 2014.

[5] M.T. Chung and C.C. Hsieh, "A 0.5 V 4.95 μW 11.8 fps PWM CMOS imager with 82 dB dynamic range and 0.055 % fixed pattern noise," in Proc. IEEE ISSCC, Feb. 2012, pp. 114–116.

[6] K. Niitsu, M. Sakurai, N. Harigai, T. J. Yamaguchi, and H. Kobayashi, "CMOS circuits to measure timing jitter using a self referenced clock and a cascaded time difference amplifier with dutycycle compensation," IEEE J. SolidState Circuits, vol. 47, no. 11, pp. 2701–2710, Nov. 2012.

[7] K. Niitsu *et al.*, "A clock jitter reduction circuit using gated phase blending between selfdelayed clock edges," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2012.