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A Low Power Data Sampling Asynchronous Power Gating Double Edge Triggered Flip-Flop

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Abstract— A low power consumptions and energy efficient method is a major role of sequential circuit design. Power gating techniques is a new technique for used to a reducing the static power consumption's of idle modules. A usage of Dual Edge Triggered Flip-flop is an efficient technique it consumed the clock frequencies and then lowers power than Double Edge Triggered Flip-flops (DETFF'S). Integrating power gating method technique DETFF is reducing the power consumption's and leakage power, further but it leads to an asynchronous data sampling problems. In these articles having two methods having to use an eradicating the asynchronous data sampling problems and their power analysis has been estimated. In order to reducing the leakage power consumption's and new designs has proposed for DETFF. Based on these new designs, of the two methods have been implemented in using 140 μm cadence tools.

Index Terms — Double Edge Trigger Flip Flop, Clock Gating, Power Gating, Single Edge triggered Flip Flop.

I. INTRODUCTION

Power efficiency and energy savings is normally considered too been a vital issue for designers. Normally, high performance chips will have a high clock frequency, which lead to high power consumptions. Therefore a less power consumed designs are needed. The major source of power consumptions in sequential circuit is a clock tree and the timing components. Higher speed of clock increased into level of integrations and technologies scaling a reasons for a high increases in power consumption. Therefore low power consumptions are becoming to very crucial factors for VLSI circuits. Performance assessments of the Space Vector Modulation showed in leak sizes, locations is both predicted with are reasonable degree of accuracies [1].

The location prediction limits of the locations sets need to be considered when searching for a leak, thereby providing a useful information's for authority. A set of novel D - type double edge triggered flip flops which can be implemented with fewer transistors than any previous designs [2]. The analysis includes an implementation independent study on the effects of input sequences, in these energy dissipations of single and double edge triggered flip flop. The system level energy savings possible by using registers consisting of double edge triggered flip flops instead of single edge triggered flip flops [3].

The requirements of an energy dissipating power high density circuits and to extend the battery life's in portable systems such as device with wireless communications capability. Flipflops are mostly power energy consumed devices [4].

Significantly amount of energy is wasted to conservatively ensured power synchronizations among them different components. A sequential circuit by a quaternary variables and used this representation to propose and analysis two clock gating technique. Based on its two types of clock gating were introduced to form a derived clock [5,6]. A new simulation and optimization approach is represented for a high performance and power issues. The analysis of an approach method reveals that sources of performance and power, a set of consistent analysis approach and simulation conditions has been introduced [7].

Flip-flops used new different types of gating techniques that reduces power dissipation to deactivating the clock signals. To overcome the presented clock duty cycle limitations of previously reported gated flip-flops. Numerical simulations of the circuits extracted from their layout with the inclusion of parasitic, show that a significant power dissipation reductions is obtained if input signal switching activity is low [8]. The power consumption of clock systems is one of the main sources of power dissipation, typically 20% to 45% of total a chip power. Consequently many ingenious techniques have been proposed a recently to reduce the clock powers of their flip flops [9].

A low swing clock double edge triggered flip flop (LSDFF) is developed to reduced power consumption significantly compared to conventional flip flops. The internal node transitions to reducing power consumption; in additions to the clock tree is reduced. The Double pulse double edge triggered flip flop uses a split output latch clocked short pulse train [10]. Compared to the previous report double edge triggered flip-flops, The DPDET flip-flops uses only a six transistors with two transistors being clocked, operating correctly under a low level supply voltage [10].

In the modern VLSI gating process the clock tree designs tends to dominates measurement must keep been taken to an under control. The design methodology has been fully integrated to an industry strength design flow, based on synopsis design compiler (front-end) and Cadence Silicon Ensemble. The performance of power characterization of DETSE includes the effect of clocking at halved the clock frequency and to impact of load imposed by the storage element to the clock distribution networks. A class of dual edge triggered flip flops with clock load, delay, and internal power consumption is comparable to faster single edge triggered storage element (SETSE) [11, 12].

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II. EXISTING METHOD

A. D Type Flip Flop

The methodology of leakage power reductions is categorized into a two classes depending on whether they reduce standby or runtimes leakage. Several techniques have been proposed they standby leakage power reduction. Variable threshold voltage MOS techniques adjust the devices threshold voltage by body biasing. Multi threshold CMOS (MTCMOS) techniques uses low voltage devices to implements main circuit elements, and high voltage devices to implements switches to disconnecting the main circuit from supply line into the standby mode. The proposed circuits deploy that reduced swing clock and data to managed dynamic powers. Furthermore, it employs clock gating and power gating process during idle modes to it's eliminates dynamic power and reduce static power, while retaining its state.

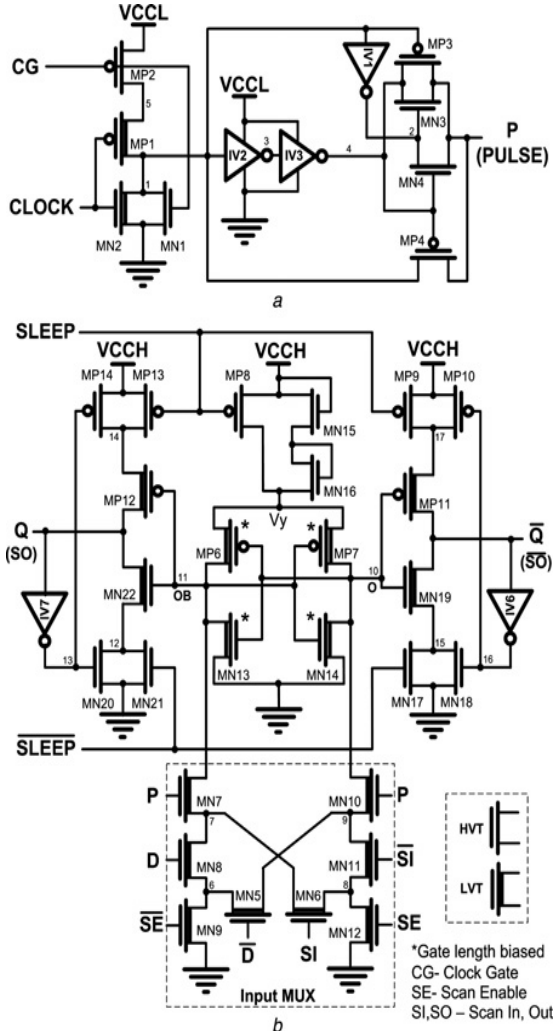

Fig .1 Single Edge Trigger Flip Flop

The static structure of the circuits makes it feasibly to be used in variable frequency power control designs. The proposed circuits used to were constructing a new low-power dual edge triggered state retention scan Flip flop called DET_SRSFF.

The proposed Flip flop reduces the static and dynamic power consumptions in both the idle clock tree and the FFs. For continuous operations of DET_SRSFF between the idle active modes, a special buffer called leakage feedback. The buffer is used to avoid floating output nodes, and the same times to hold the states of the Flip flop idle mode. The overall Process Dynamic Power of DET_SRSFF is comparable with conventional high performance Flip flops at the same time with extra level conversion and state retention features.

B. Clock Gating

A double edge triggered half static clock gated D-type flip-flop (DHSCGFF), which consists of two parallel dynamic master latches connected in a parallel single half static latch with clock gating circuit. The proposed DHSCGFF makes use of a clock gated circuits to achieved better race tolerance, circuit compactness and energy efficiency without their use of pulse generator. A simulation result of proposed circuit using a 0.18 nm technology is presented. The proposed circuit double edge triggered half static clock gated D Flip flop (DHSCGFF).

The core of the flip-flop is shown in Fig. 1 (b), which consists of two identical dynamic master latches and a half-static slave latch. Compared with the SET implementation [3], the proposed DHSCGFF consists of an additional master latch (master latch 2 in Fig. 1) in parallel to the original master latch. The proposed DHSCGFF also makes use of a clock-gating circuit to suppress the redundant transitions and achieves 96%. Reduction in redundant power dissipation at 0; = O. Since no pulse generator was used, the timing flexibility of the circuit can be maintained.

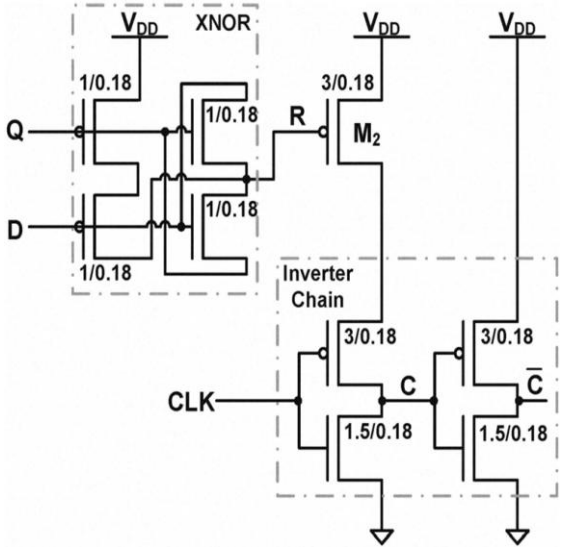

Fig .2 Clock Gating Circuit

C. Clock Gating Circuit

The proposed DHSCGFF does not require any pulse generator; it reduces the power dissipated on the clock network. The efficiency of the proposed DET-FF can be

further enhanced by introducing a clock-gating circuit. This simple and energy efficient clock-gating circuit is based on XNOR circuit constructed by pass transistors [8]. The pass transistor logic simplifies the circuit and reduces the internal power dissipation.

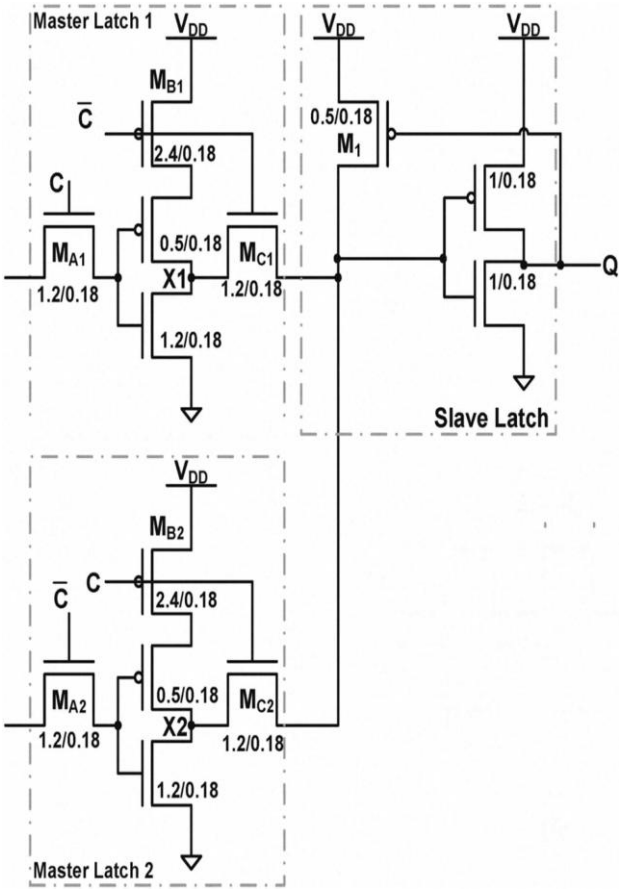

Fig .3 Master Slave Flip Flop

III. PROPOSED METHOD

Power Gated D Flip-Flop

The pulse generator is used which produce the dual pulse which is active at both rising and falling edge of the clock. The C (internal gated clock) signal maintains its value instead of generating an active edge in the gating mode. C changes after the transition on CLK in the non-gating mode.

Asynchronous data transition occurs in DET_SRSFF, when there is an input change while CLK equals 0. Because when there is a change in the input, clock signal is made inactive. At that time when the input is stable that means no significant change in the output. But still at that time circuit evaluate the input. This is basically used to control the discharge path. The dual triggered pulse generator produces a brief pulse signal synchronized at both rising and falling clock edges.

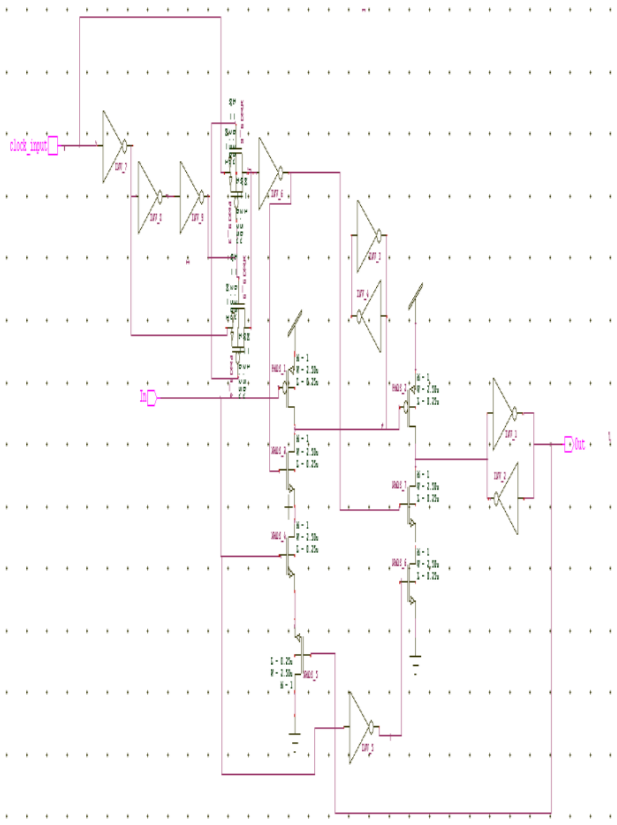

Fig .4 Existing System

Conditional precharge technique is used for removing the redundant transitions of the flip-flop to reduce the power dissipation. The schematic of this type of circuit is shown in fig 4. In this conditional technique for preventing the precharging of internal node discharging path is controlled when the input remains is high for long time. The flip-flop's output is examined and the transition is allowed only if there is a significant change in the output of the flip-flop. The correct choice of flip-flop and its corresponding design has a deep effect in reducing the power consumption. Pulse triggered flip-flops gave better output as compared master slave latch flip-flops because of timing issues.

There are different types of the dual edge triggered flip-flop used in the different synchronous circuits. There are many microprocessors which use master-slave and pulse triggered flip-flops. Master slave dual edge triggered flip flop which is made up of two stages, one is master and other is slave. They are characterized by the positive set up time and large D to Q delay. Also there is duplicating of the latch part one is for master and other is for slave. Examples of master-slave flip-flops include the transmission gated transmission gated based flip-flop, push-pull dual edge flip-flop and transmission gate latch mux (TGLM). In pulse triggered flip-flops, one is implicit pulse triggered flip-flop in which for generating the clock pulse implicit pulse generator is used and other one is explicit pulse triggered flip-flop in which generation of the clock pulse by explicit pulse generator.

IV. EXPERIMENTAL RESULTS

A. Proposed Dual Edge Triggered FF

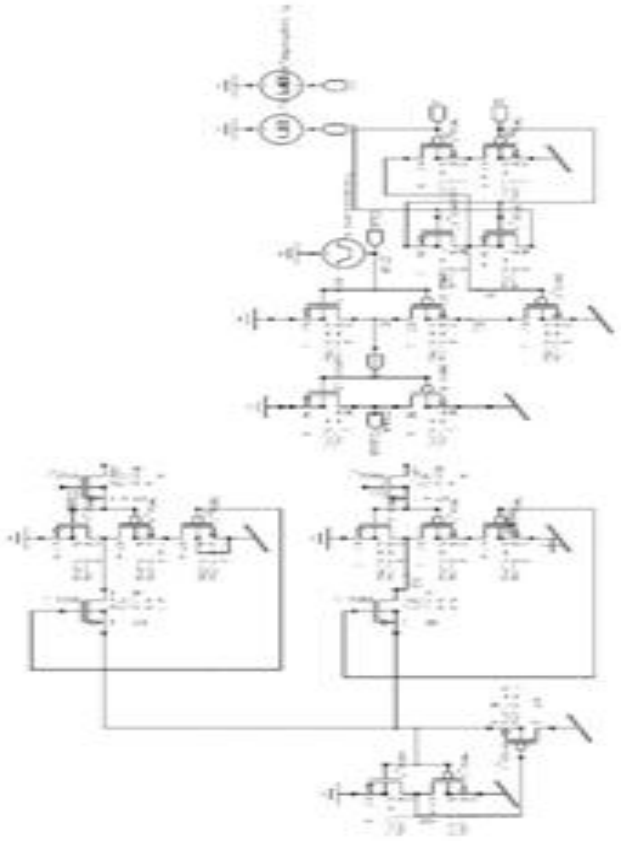

Fig 5 Schematic representation Proposed work

In this proposed circuit of flip-flop some type of controlling circuit is embedded so that clock is disabling when the input invokes no output change. In order to eliminate the redundant transitions this data dependent technique based flip-flop is proposed. This results in saving of the power because the clock is disable at the point when no significant change at output because of stable input.

V. RESULTS

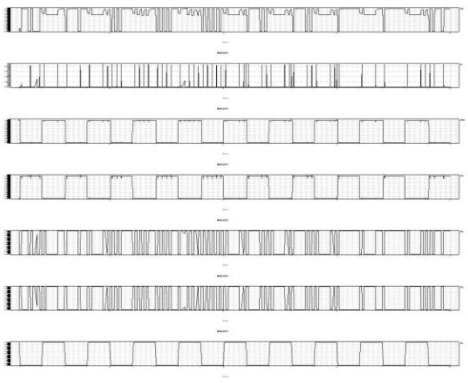

Fig 6 Simulation Output

Power Results

V1 from time 0 to 2e-006
Avg power consumed -> 1.032937e-003w
Max power 4.580270e-003 at
Time 9.29607e-008
Min power 4.637432e-009 at
Time 9.3e-007

VI. CONCLUSION

Various power reduction techniques emerged as a result of high demand in mobile devices. DETFF is an efficient technique for power reduction, when used separately. When clock gating technique is integrated with DETFF, asynchronous data sampling problem arises at the output between two clock edges. This problem has been defined in detail and solutions were given to eradicate it. Three simple approaches were made to reduce the power consumed in DETFF's by eliminating the asynchronous data sampling issue. In order to reduce the power consumption further, a new design has been proposed and based on that, three designs were implemented using Tanner EDA Tool.

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