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DESIGN OF HIGH EFFICIENT AND LOW POWER MULTIPLIER

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Abstract— Multiplication is one of the basic arithmetic operations and it requires more hardware resources and processing time than addition and subtraction. A fast method for multiplication based on ancient Indian Vedic mathematics is used in this paper. The Vedic Multiplier based on "Urdhva Tiryakbhyam" algorithm of Vedic Mathematics is designed by using GDI (Gate Diffusion Input) Technique. The multiplier circuit is optimized for energy efficiency at 130nm and 90nm CMOS technology. This multiplication is to improve the speed and power of multipliers. Further, this Vedic Multiplier can be used in matrix multiplication. The design shows excessive improvement in terms of power when compared with CMOS.

Keywords **--** GDI, HSPICE, Urdhva Tiryakbhyam, Vedic Multiplier.

I. INTRODUCTION

In VLSI design the major area of concern are high speed, small area and low power. Many applications suffer from low battery life due to absence of low power design technique. Multiplication is one of the arithmetic operations. The multiplication operation is performed by successive addition. Multiplier is a device used to perform multiplication operation. All multiplier performs multiplication operation in two steps. First step involves the process generating partial product. Next step involves the process of summing the partial products. The reliability of the multiplier is suffered by power dissipation.

Vedic mathematics is a part of four Vedas. It was re-introduced in twentieth century by Swami Bharati Krishna Tirthaji Maharaj. The word "vedic" is derived from the word "Veda" it means the store house of all knowledge. It is mainly based on 16 Sutras. The Vedic formulae are based on the natural principles on which the human mind works.

It can be applied to various branches of engineering such as computing and digital signal processing. The multiplier architecture is classified into three categories. They are serial multiplier, parallel multiplier and serial-parallel multiplier. The Vedic multiplier is implemented based on the one of the sutras. Vedic multiplication is based on the algorithm Urdhva Tiryakbhyam.

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II. GDI TECHNIQUE

The large number of function can be implemented using the basic GDI cells. GDI is the modified form of CMOS. Because of the basic cell of GDI is same as the standard CMOS inverter. The difference between CMOS and GDI, is that GDI cell contain three inputs: G, P and N. G is input to gate of the transistor, P is input to source or drain of the PMOS transistor in GDI cell. Similarly, N is input to source or drain of the NMOS transistor in GDI cell. GDI is implemented in twin well CMOS or silicon on insulator.

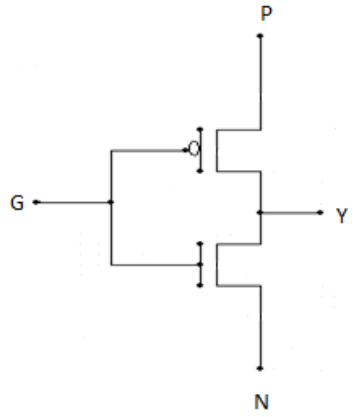

Fig 1: GDI Structure

In p-well CMOS process all the functions are not possible. But all the functions can be implemented in twin well CMOS process. The table1 corresponds to six different Boolean functions. To perform F1 operation, the inputs are N=0, P=B and G=A. To perform F2 operation, the inputs are N=B,P=1 and G=A. To perform OR operation, the inputs are N=1, P=B and G=A. To perform AND operation, the inputs are N=B, P=0 and G=A. To perform MUX operation, the inputs are N=C, P=B and G=A. To perform NOT operation, the inputs are N=0, P=1 and G=A.

Table1: Functions of GDI cell

N	P	G	Out	Function
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT
0	B	A	A'B	F1
B	1	A	A'+B	F2

III. VEDIC MULTIPLIER

The multiplier is based on Urdhva Tiryakbhyam algorithm of ancient Indian Vedic Mathematics. It literally means "Vertically and crosswise". It is used to generate all partial products and at the same time concurrent addition of these partial products can be done. Thus, it produces products by parallelism. The algorithm can be used for nxn bit number.

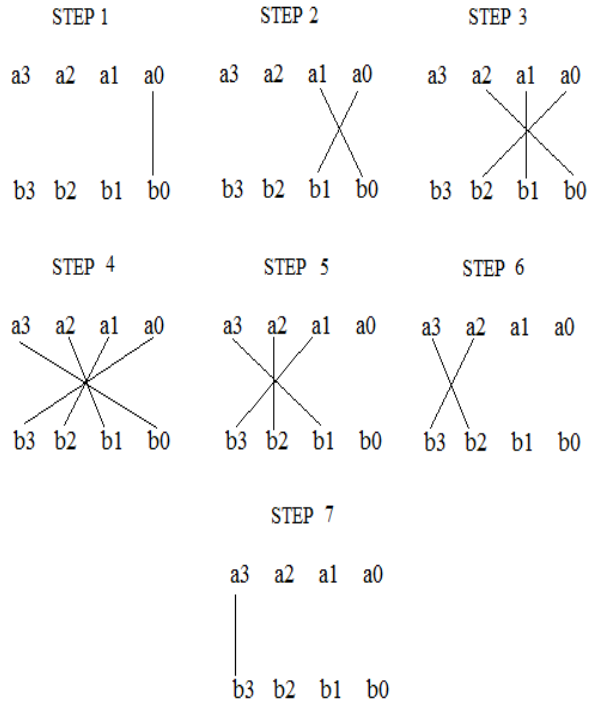

Fig 2: Parallel calculation Methodology

The above figure 2 shows the parallel calculation methodology for 4x4 Vedic Multiplier. As the partial products and their sums are calculated in parallel, multiplier is independent of the clock frequency of the processor. As the number of bits increases, the gate delay and area increases very slowly when compared to other multipliers and this forms the greatest advantage of this multiplier. It enhances the ALU unit. The 2x2,4x4 and 8x8 bit Vedic multiplier module are displayed in the below sections. The Urdhva Tiragbhyam sutra is used for the multiplication of the binary number. The Vedic multiplier is well adapted to parallel processing.

IV. 2X2 VEDIC MULTIPLIER

The block diagram of 2x2 bit Vedic multiplier is shown in figure. The 2x2 Vedic multiplier has two inputs having two bits each and are: A=a1a0 and B=b1b0. The LSB of the multiplier is multiplied with LSB of multiplicand gives the product as S0 (a0b0). The LSB of the multiplier is multiplied with MSB of the multiplicand is summed with MSB of the multiplier is multiplied with LSB of the multiplicand gives the product as S1(a1b0+b1a0).

The MSB of the multiplier is multiplied with the MSB of multiplicand and gives the product as S2 and carry of second half adder becomes the fourth bit of the final product.

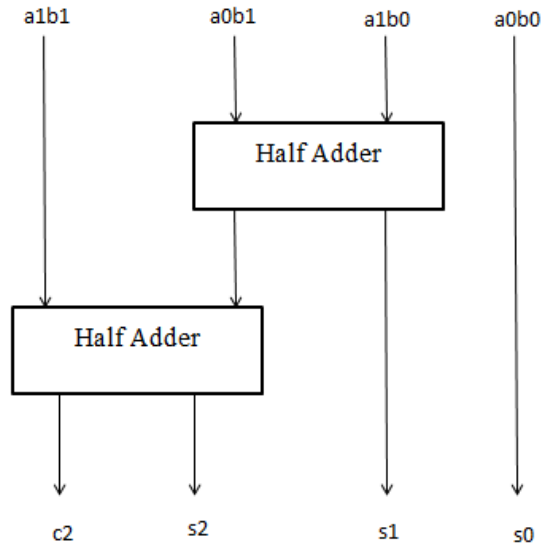

Fig 3:2x2 Vedic Multiplier architecture

V. 4X4 VEDIC MULTIPLIER

The block diagram of 4x4 Vedic multiplier is shown in figure. The 4x4 multiplier has four AND gates, four 2x2 Vedic Multipliers and three four bit Ripple carry adders.The 4x4 Vedic multiplier has two inputs having four bits each and are: A=a3a2a1a0 and B=b3b2b1b0 and gives the products as S0 S1 S2 S3 S4 S5 S6 S7.The arrangement of Ripple carry adder is used to reduce the delay and increases the speed.

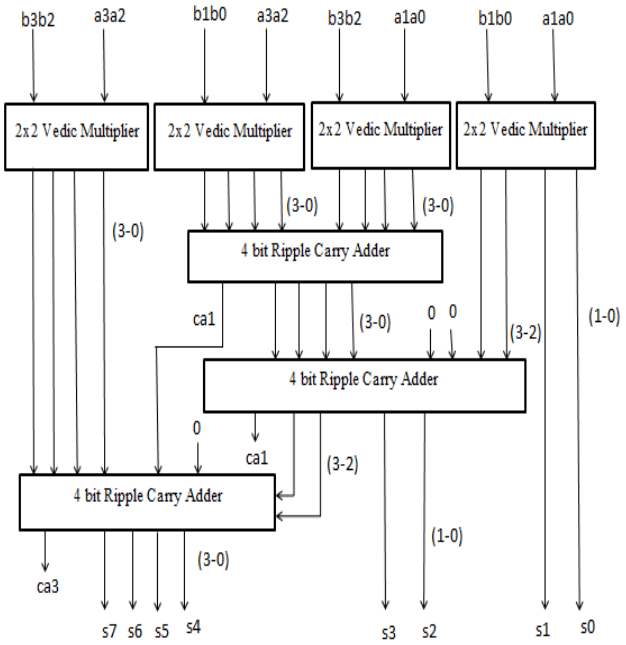

Fig 4: 4x4 Vedic Multiplier architecture

VI. 8X8 VEDIC MULTIPLIER

The block diagram of 8x8 bit Vedic multiplier is shown in figure. It can be easily implemented using four 4x4 bit Vedic multiplier and three 8-bit Ripple carry adder. The 8x8 bit Vedic multiplier has two inputs having eight bits each. Where, A=a7 a6 a5 a4 a3 a2 a1 a0, B=b7b6b5b4b3b2b1b0 and the products are S0 S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15.The result will be of sixteen bit.

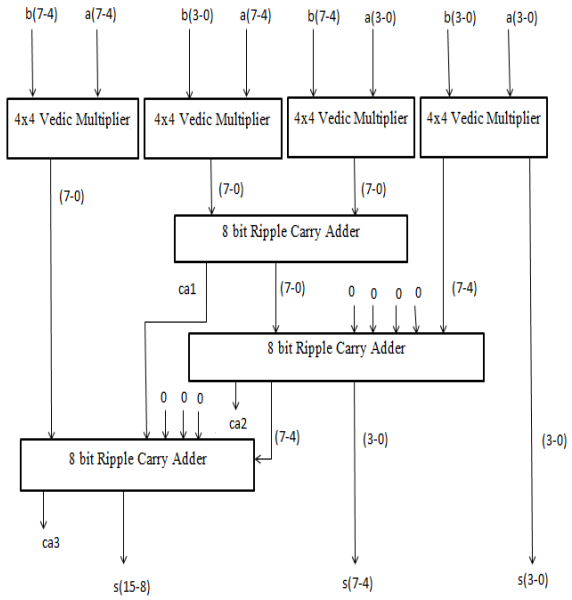

Fig 5: 8x8 Vedic Multiplier architecture

VII. SIMULTATION AND RESULT

Basic GDI Function has been simulated using HSPICE. A novel GDI technique for low-power design was implemented in Vedic Multiplier and the technology being used is 130nm CMOS digital technology. The simulated outputs are shown below.

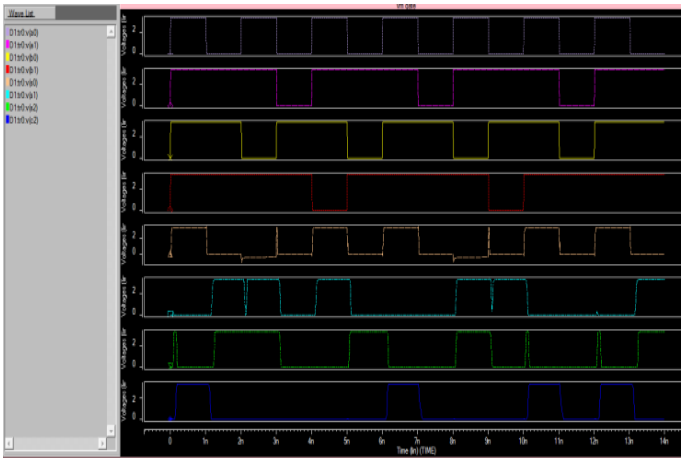

Fig 6: Output of 2x2 Vedic Multiplier

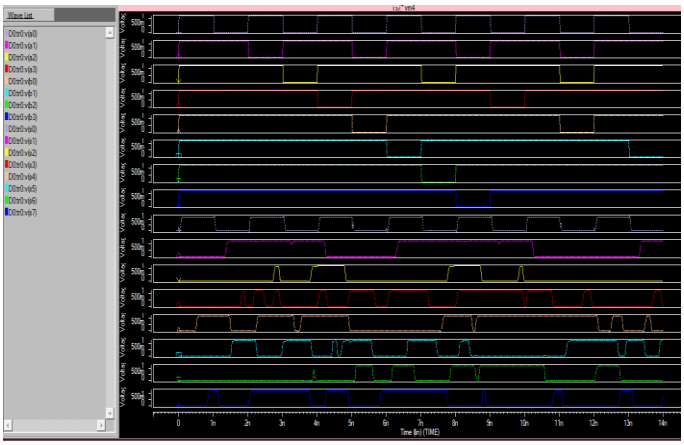

Fig 7: Output of 4x4 Vedic Multiplier

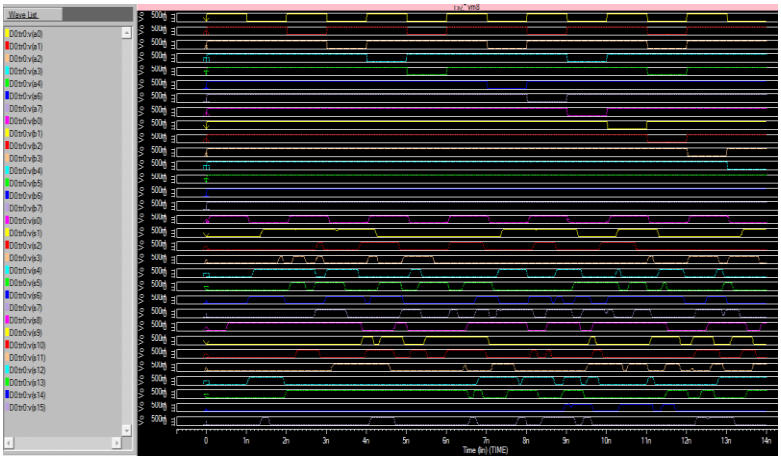

Fig 8: Output of 8x8 Vedic Multiplier

VIII. CONCLUSION

The Vedic Multiplier using GDI (Gate Diffusion Input) structure is designed for Low Power applications. The proposed multiplier successfully operates at low voltages with tremendous signal integrity and driving capability. The proposed design not only reduces the power but also increases the speed. Thus GDI can be used to reduce the power dissipation of the digital systems. The multipliers design is compared with both 90nm and 130nm technologies and in 90nm technology the power is further reduced.

Hence, GDI technique can be used to design low power circuits such as digital wrist watches, radio frequency identification (RFID),sensor nodes, laptops, pacemakers and battery operated devices such as, cellular phones etc., The above combinational circuit design can highly fill place for the sequential circuit design for providing a better design. In low power VLSI design GDI technique has very good scope for future.

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