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Ds-Cdma Multiuser Receiver Employing Iterative Multiple Access Interference Cancellation

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Abstract— Interference plays a crucial role in performance disturbance in communication networks. To avoid from the interference there are many different techniques for different cases. This paper proposes an implementation of Direct Sequence-Code Division Multiple Access (DS-CDMA) for Multiple Access Interference (MAI). MAI is a factor which limits the capacity and performance of DS-CDMA system. Multiple Field Programmable Gate Array (FPGA) platforms and multiple technology nodes for synthesized Application Specific Integrated Circuits (ASIC) results are presented here. For combined interference detection is performed using the generalized version of Interleave-Division Multiple-Access (IDMA) known as Partition Spreading (PS) CDMA. Decoding is performed using two iterative methods turbo and sum-product decoding. The synthesized ASIC system demonstrates a maximum aggregate throughput of 197 Mb/s for a fully loaded 50-user system, while the implemented FPGA 50-user system has a maximum aggregate throughput of 119 Mb/s.

Keywords —Interference cancellation, partition spreading, field programmable gate arrays, Direct-sequence code-division multiple access, digital circuits, space-frequency block codes.

I. INTRODUCTION

One approach to creating flexible and spectrally efficient multiuser wireless communication system is to use Direct-Sequence Code Division Multiple Access (DS-CDMA) technology. Instead of dividing the available spectrum into time or frequency slots the user are separated by unique pseudorandom signature sequence that spread their signal across a frequency range. In direct sequence transmission using CDMA, the user data is multiplied by a sequence of codes usually binary sequence are used.

The duration of an element in the code is known as 'chip time'. The ratio between the user symbol and chip time is known as spread factor. The signal to be transmitted occupies a bandwidth which is equal to the spread factor times the bandwidth of user data. The signals are decoded using the same unique sequences at the receiver in correlation front-end. The code sequences are pseudo noise sequence, Walsh Hadamard codes, Gold codes and Kasami codes. Here pseudo sequences are used. A major difficulty in Direct Sequence transmission is the Near Far effects. If more than one user is active then the incoming interference power is suppressed by cross correlation between the code of reference user and the code of interferer.

In the event path the interferer is closer to the receiver than the reference user. The interference components cannot be sufficiently attenuated by the dispreading process. In the cellular CDMA systems, adaptive power control [1] is used to avoid the near far effect.

Wei-Xiao proposed complementary Coded Code Division Multiple Access (CC-CDMA) [2] systems in frequency selective fading channels. Pre-carrier parallel interference cancellation technique is used based on Mean Square Error Combining (MSEC) to achieve a frequency diversity gain multiple user interference resistance. A conventional DS-CDMA system treats each user separately as a signal, with other users considered as noise or MAI.

The optimal MAI detector is impractical for implementation since its complexity increases with number of users. The suboptimal detector performance is better than the conventional detector but with lower computational complexity than the optimal detector. The suboptimal detector are Parallel interference cancellation (PIC), Successive Interference Cancellation(SIC),Space Alternating Generalized Expectation (SAGE) and partition spread(PS)-CDMA.

Binary Phase Shift Keying (BPSK) is a key technology for modulation and signal propagation. Interference cancellation represents the remarkable role in modern receiver designs for wireless communication networks. Parallel Interference Cancellation (PIC) for single and multiple antenna systems also proposed. SIC is an effective way of multiple packet reception to minimize interference in wireless networks [5]. The capacity of modern wireless communication system is interference limited. This investigates the scheduling performance in wireless networks with SIC. It successively subtract off the strongest remaining signal. Cancelling the strongest signal has the most benefit and most reliable cancellation.

Parallel Interference Cancellation (PIC) [6] is an attractive decoding scheme for Multiple-Input Multiple-Output (MIMO) wireless communications. It simultaneously subtract off all of the users' signals from all of the others it works better than SIC when all of the users are received with equal strength (e.g. under power control).

Known interference cancellation schemes are also introduced called Blind Known Interference Cancellation (BKIC) [10] are also proposed with good performance and low complexity. For multipath interference cancellation in broadband signals, novel optical technique [11] is used. Multiple optical compensation branches are used to remove wireless multipath effects.

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The duplicated signal is subtracted from the total received signal to recover the signal of interest while suppressing interference. Adaptive interference cancellation method [12] is used by Moonchang for cancelling the self-mixed interference. Polar Codes [13] proven to achieve symmetric capacity of any binary-input discrete memory less channel.

The Successive Cancellation List (SCL) decoding and the Successive Cancellation Stack (SCS) decoding [14] are used to improve the finite length performance of polar codes. This algorithm provides a flexible configuration when the time and space complexities are limited. Yung-Yi presented the Carrier-Frequency-Offset (CFO) [16] estimation algorithm for time dispersive orthogonal frequency division multiplexing system using the general inter-carrier self-cancellation scheme.

In cellular uplink DS-CDMA is presented by Don Torrier [15] using variable power control that allows an outage constraint to be enforced on every link, which is impossible when a fixed rate is used through the network. Previously introduced Partition Spread (PS)-CDMA is used in this paper. PS-CDMA is a general approach to Interleave Division Multiple Access (IMDA). It is popular technology due to its simple construction and iterative nature. In PS-CDMA we take the view so that Direct Sequence Spread Spectrum (DSSS) signal can be viewed as a repetition code.

One important property of the air interface of a cellular telephone system is the multiple access method. Each user of the cellular system is given a channel, and all users get different channels. The way in which these channels are different is determined by the multiple access method.

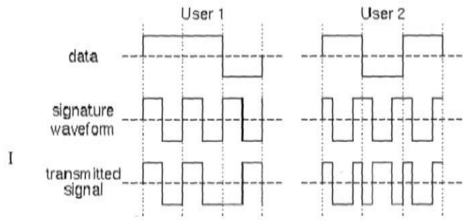

Fig.1 CDMA

In a cellular system employing Direct Sequence Code Division Multiple Access, all users use the same frequency at the same time. Before transmission, the signal from each user is multiplied by a distinct signature waveform. The signature waveform is a signal which has a much larger bandwidth than the information bearing signal from the user.

All users use different signatures waveforms to expand their signal bandwidth. The procedure is depicted in figure 1 for a two-user case. Notice the phase shifts in the transmitted signal is due to the negative pulses in the data stream. Since bandwidth is a limited resource, one of the primary design objectives of all modulation schemes is to minimize the required transmission bandwidth. Spread spectrum techniques on the other hand employ a transmission bandwidth that is several orders of magnitude greater than the minimum required signal bandwidth.

II. System Model - Transmitter And Detector

DS-CDMA system model using Binary Phase Shift Keying (BPSK) modulation is used. Figure 2 shows the transmitter block diagram for each user.

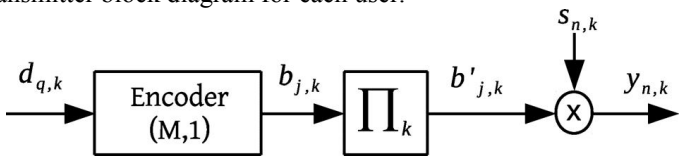

Fig.2 PS-CDMA transmitter diagram with effective repetition coding and interleaving of partitions.

At the transmitter encoded bits of user (could be the result of high-rate LDPC encoding as this detector performs very well in conjunction with high rate codes) are encoded by a repetition code as part of the DSSS modulation operation. In coding theory, the repetition code is one of the most basic error correcting codes. In order to transmit a message over a noisy channel that may corrupt the transmission in a few places. The idea of the repetition code is to just repeat the message several times.

Typically is chosen between 3–5 as larger values have limited additional effect on performance. The resulting coded bits, $b_{j,k}, j \in \{1, \ldots N_{m,}\}N_{m=LM}$ are interleaved by a user-distinct interleaver $\pi_k$to obtain $b'_{j,k}$. Since the system uses DS-CDMA, the interleaved coded bits are spread by a user-distinct spreading code $s_{j,k}$. These spreading codes have a reduced length, or processing gain of N/M, with respect to the baseline CDMA system which would use spreading sequences of length N. This normalization is used to ensure fair power and spectral comparisons. Before transmission, each user has a power P_k assigned to it and its chips are normalized to the overall (uncoded) spreading gain N, i.e., $c_k = 1/\sqrt{N}$. Using BPSK the System Load (SL) is a key parameter for comparing performance of different systems.

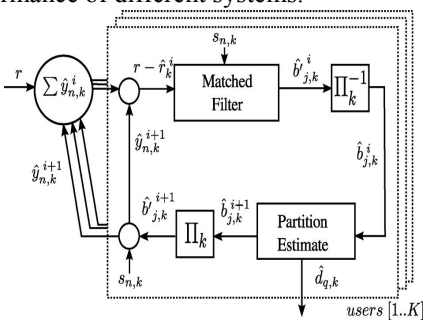

Fig.3 Block diagram of the demodulation operation of the PS-CDMA receiver

Figure 3 shows demodulation operation of PS-CDMA receiver which consists of K parallel individual data receivers with the single users' processor path outlined with a dash box.

The receivers decode their respective transmission embedded in r and then in parallel share their estimate with each other to attain an interference reduced version of r. All the users' signals y_j aggregate in the AWGN channel to give the received signal shown in Equation 1.

$$r_j = \sum_{k=1}^{K} Y_{j,k} + n \quad (1)$$

Where n is the contribution of the additive white noise this assumption is not critical for either performance or implementation complexity of the decoder itself. Here the estimate of each received signal $y^i_{j,k,n}$ at the chip level is summed to approach an interference free estimate of the received signal at the i^{th} iteration of processing. The first iteration has no estimates available and skips the cancellation stage. To attain an estimate of the user's transmitted partitions the conventional matched filter is used to correlate the unique signature sequences $s_{j,k}$ with the incoming noisy waveform to give sufficient statistics of the user's signals.

By the analysis it is seen that for a given SL, the absolute size of the systems does not affect the Bit Error Rate (BER) of the interference cancellation appreciably at high system loads. To attain an estimate of the user's transmitted partitions, conventional matched filter is used to correlate the unique signature sequences with the incoming noisy waveform to give sufficient statistics of the user's signals.

III. System Architecture

FPGA and ASIC implementations are presented. C++ is used for design parameters for BER performance and performs bit true calculations. The transmitted signal is stored in memory. The memory is shared to all receivers as the data is streamed to all receivers simultaneously. Chip arrival between all users is assumed to be synchronous. Figure 4 shows the Architecture of the PS-CDMA iterative demodulator. The PS-CDMA with iterative decoding can approach both performance of optimal detection of CDMA and also the capacity of the CDMA channel if used together with spatial coupling.

Architecture Of Proposed System

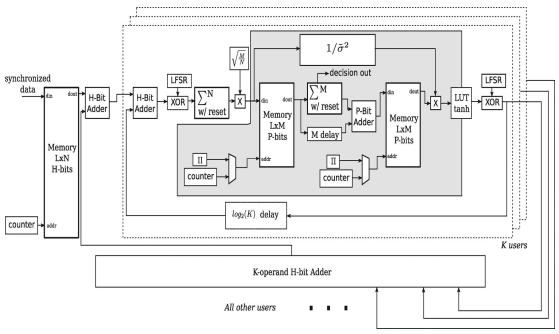

Fig.4 Architecture of the proposed iterative demodulator for PS-CDMA

A. Matched Filter

Matched filters are a basic tool in electrical engineering for extracting known wavelets from a signal that has been contaminated by noise. In the context of a communication system that sends binary messages from the transmitter to the receiver across a noisy channel, a matched filter can be used to detect the transmitted pulses in the noisy received signal. The matched filter is the optimal linear filter for maximizing the Signal to Noise Ratio (SNR) in the presence of additive stochastic noise. The current CDMA receivers are based on conventional detector, also known as matched filter.

In conventional single user digital communication system the matched filter is used to generate sufficient statistics for signal detection. The detector is implemented as a K separate single-input (continuous-time) single-output (discrete-time) filters with no joint processing at all. Each user is demodulated separately without taking into account to the existence of other (K-1) active users in the system. In other words, other users are considered as interference or noise. The exact knowledge of the users' signature sequences and the signal timing is needed in order to implement this detector. Chip arrival between all users is assumed to be synchronous, so the matched filter consists of an gate, an accumulator (with reset), and a scaler. The scaler multiplies the partitions by $\sqrt{M/N}$.

The takes advantage of the sign-magnitude form by tying the output of the linear feedback shift register (LFSR) with the most signi ficant bit (MSB) of the data. This avoids the need for multiple bit switching that two's complement would require. The design of the matched filter is shown in Fig.5

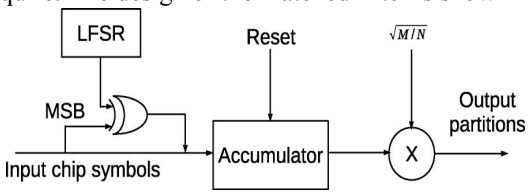

Fig.5 Matched filter block diagram

The LFSR is a 51 stage delay line, with stages 1 and 4 tapped. The value of each stage is programmed to a unique sequence for each user. The length and taps were chosen to supply a suitable pseudo-random number generator

In the matched filter a transition between two processing domains occurs. The chip processing domain requires a greater precision in data representation. While partition processing domain requires less precision. The first path forms estimates the data and calculate hard decision while second path is used to form an estimate of the variance in the signal. Each received partition element after matched filter with its individual spreading sequence is given as

$$b^i_{j,k} = \sum_{n=1}^{N/M} (r_n - r^i_{k,n}) s_{j,k,n} \quad (2)$$

Equation 2 contains the contributing elements to the partition estimates as the detector iterates. With adequate Signal-To Noise Ratio (SNR) the chip samples $y^i_{j,k,n}$ approaches the value of $y_{j,k,n}$ meaning the interference $I^i_{j,k,n}$ goes to zero with iterations. The Log-Likelihood Ratio (LLR) of at iteration is computed is as in Equation 3

$$\log\left(\frac{p_r(d_k=1)}{p_r(d_k=0)}\right) = \frac{2}{\sigma^2}\sum_{j=1}^{M} b^i_{j,k} \quad (3)$$

B. Interleaver

Interleaver has a depth of L*M elements. Instead of storing the indices, they are calculated in order to reduce the

usage of memory. Serial implementation is chosen but design can also operate in parallel.

Polynomial being used is

$$(63x+128x^2+h) \bmod (L*M). \quad (4)$$

The interleaver implemented in FPGA relies on available Block Random Access Memory (BRAM). The sequential design introduces latency since the entire frame must be written in to memory.

C. Partition Estimation

In the implementation, shown in Figure 4 the partition estimation is split around the interleaver. The tanh step of the estimation operation is separated from the extrinsic step in order to give the system a chance to develop an estimate on the variance statistic used to weight the tanh operation. The extrinsic step uses an accumulator and a delay element (flip-flops). A partition is delayed by M cycles so that the M partitions of a symbol can be accumulated. Then the partition is subtracted from the sum, to attain the extrinsic partition. This occurs for all M partitions in the delay pipeline. By looking at the MSB of the accumulator's sum hard decision for the iteration is obtained.

D. Variance Calculation

The variance is calculated assuming that the partitions of the matched filter give the correct hard decision. The variance is calculated by using Equation 5

$$\frac{1}{\sigma^2} = \frac{\Sigma}{N} = \frac{LN}{\sum_1^{LN}(y_k - \frac{1}{\sqrt{3}})} \quad (5)$$

The sliced variance operation is performed using series of shifts with a multiplier and an accumulator followed by a Look Up Table (LUT). The LUT performs the $1/x$ function to weight the extrinsic partitions. All K users' chip estimates are aggregated and subtracted from the original received signal. If the estimates are perfect, the only values left are the contribution of noise to that chip.

IV. CANCELLATION

The final stage of receiver creates an estimate of the transmitted signal. The result from the decision operation is sign extended to H-bit signal for the cancellation operation. Before cancellation, the chips are first delayed by 1/sqrt(N) and then scrambled with the appropriate spreading sequence. In order to align them with the transmitted values.

A main component of receiver is common aggregator that sums all K users estimate in order to cancel the interference. In this implementation full adder tree is used. The implementation results for the FPGA and ASIC are compared. Each user has the same power which is a worst case for this case. The overall system size doesn't affect the BER performance as long as the system load remains constant. To track the number of iterations a counter is also used. The FPGA result gives the significant reduction in control logic and cancellations operations.

Instead of mapping interleaver memory to SRAM, the memory is mapped to registers consisting of positive edge of D-flip-flops. This is done to avoid from the implementation of memory controller. The ASIC design complexity can also be reduced by changing the interleaver address generator to architecture.

V.SIMULATION RESULT

The implementation results for FPGA are summarized in this section. VHDL simulation and FPGA implementation was confirmed using ModelSim.

A. Simulation Result of Matched Filter

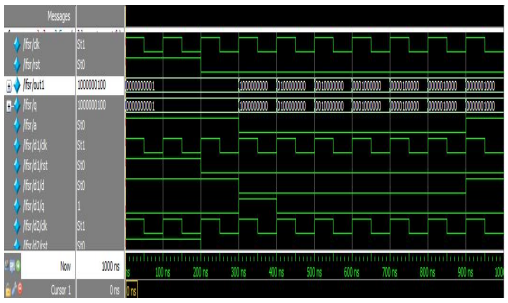

Figure 6 Simulation result of matched filter

To attain an estimate of the users transmitted partitions use a conventional matched filter to correlate the unique signature sequence with incoming noisy waveform to give sufficient statistics of the users signal. In PS-CDMA detector K matched filter operate on the received chip to generate soft partition for each user.

These estimates are used in a similar fashion to sum-product decoding to attain extrinsic estimates, which are iteratively calculated to cancel out the multiple access interference.

In the matched filter a transition between two processing domains occurs, the Chip processing domain and the partition processing domain. The chip processing domain requires a greater precision in data representation of H-bits, while the partition processing domain requires a less precise representation of P-bits.

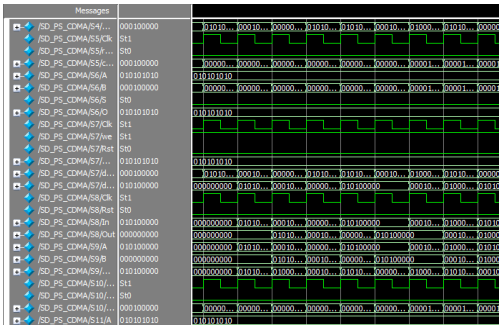

Figure 7 Simulation result of partition estimation

This occurs due to the soft processing that occurs in the tanh-limit, whereas the cancellation requires a precision that can handle fractions of transmitted amplitudes. After the matched filter the data takes two parallel paths. The first path forms estimates of the data and calculates hard decisions. The second path is used to form an estimate of the variance in the signal.

B. Simulation Result of Partition Estimation

The partition estimation is split around the interleaver module. If partition is veiw as a separate estimate of the original data symbol it can sum the M partition and take the sign of the sum as the hard decision of the detector output. In order to perform the partial interference cancellation of chips must recreate them identically to the user's respective transmitted signal.

All K users' chip estimates are aggregated and subtracted from the original received signal. If the estimates are perfect, the only values left are the contribution of noise to that chip. For the tanh step, use a small look-up table with P-bit inputs and H-bit outputs that have also moved the scaling from cancellation into LUT to avoid an extra multiplier.

C. Simulation Result of Proposed System Output

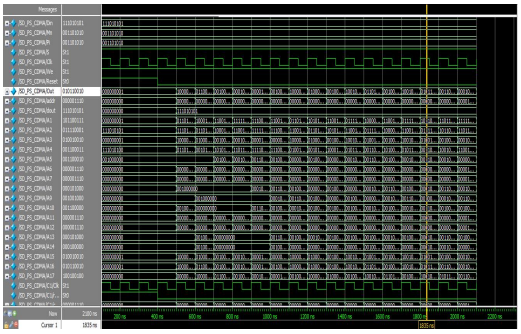

Figure 8 Simulation result of proposed system

Implementation was found to have acceptable performance using P=8 and H=11 on their respective data paths. The system latency is determined by the number of iterations needed to reach the target BER. The detector has specific parameters that limit the number of user implementable and other limitation to the design is the serial nature of the interleaver and their impact on memory usage and throughput. The significant logic reduction can still be made within the control logic and cancellation operation. This indicates that future implementations may attain more users and therefore a higher aggregate throughput.

VI. CONCLUSION

Joint detection iterative interference cancellation technique is implemented in this article. Many other cancellation techniques are also discussed with a brief introduction. The proposed technique base unit of the architecture is comprised of a few simple components. But this allows large system implementations and giving good performance. DS-CDMA technology is used to create flexible and spectrally efficient wireless communication system. The variance module, control module and cancellation modules were identified as logic blocks that could be reduced in their logic requirements. The serial nature of the interleavers was identified as a bottleneck for the throughput and major contributor to implementation area.

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